SERIES 35 PLUS

Operator's Manual

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Series 35 PLUS
Operator's Manual
Publishing History

Manual Version	Changes Made	Date	Firmware Version
1.0	First release	April, 1984	V1.0
1.1	Corrections	September, 1984	V1.0
1.2	Expand section 1; reorganize sections 6 and 7 for clarity; add figures 5.3 and 5.4; add index	January, 1985	V1.0

PREFACE

The Series 35 PLUS Operator's Manual is organized so that it can be used by both the experienced MCA operator and the newcomer to nuclear analysis. It is divided into ten sections for easy reference:

1. An introduction to the Series 35 PLUS Multichannel Analyzer and a basic description of the two main modes of operation--PHA and MCS.

2. Basic operating rules for the Series 35 PLUS.

3. Two simple experiments to show how to use the PHA mode and the MCS mode.

4. A description of the front panel controls.

5. Data input and output.

6. The Task (learn/execute) function.

7. The Define/Use/Ap-Pak options.

8. The Models 3543 and 3544 Analysis options.

9. Standard and optional wiring.

10. Signal processing options.

The experienced MCA operator can proceed directly to Sections 2 and 4 through 10 to learn the specific functions of the Series 35 PLUS MCA. The less experienced operator should study the first sections before attempting more than the most basic use of the analyzer. Sections 4 through 10 assume a working knowledge of Sections 1, 2 and 3.

CLEANING THE FAN FILTER

The fan filter at the rear of the Series 35 PLUS must be cleaned periodically (every month or so, depending on the environment) to assure a flow of cooling air to the interior of the analyzer.

If the internal temperature of the Series 35 PLUS is allowed to rise above a safe level, a thermal cutout will remove power from the Series 35 PLUS to allow the temperature to go down.

To clean the filter, remove the four wing nuts holding it in place, then pull it off the mounting studs. Be careful not to bend the filter's aluminum frame.

The filter may be cleaned by brushing, by blowing with compressed air or by washing. If the filter is washed, be certain that it is completely dry before replacing it in the analyzer.

After cleaning the filter, put it back on the mounting studs and replace the four wing nuts. Tighten the nuts securely to prevent the fan's vibration from loosening them.

CLEANING THE MONITOR

A high-voltage induced static charge on the face of the display monitor can attract dust. To remove the dust, clean the face of the monitor with a soft cloth dampened with water. Note that the area being cleaned is a plastic anti-glare filter; take care not to scratch it.

To avoid further static charge accumulation while wiping the screen, hold on to the frame of the Series 35 PLUS while cleaning the display.

SECTION 1
INTRODUCTION TO THE SERIES 35 PLUS

The Series 35 PLUS consists of a master controller and five sections: memory, display, signal processing, operator/MCA interface, and data input/output. The controller is a microprocessor which reads its instructions from a permanent program in the memory; it controls the MCA functions and directs the use of the 3500 bus.

1.1 MCA Sections

The two part memory section consists of the preprogrammed Read Only Memory (ROM), which contains the microprocessor's instructions (firmware), and the Random Access Memory (RAM), which stores the operator's instructions and the acquired data.

The RAM is powered by an internal battery which allows data and parameters to be retained when the ac power is off.

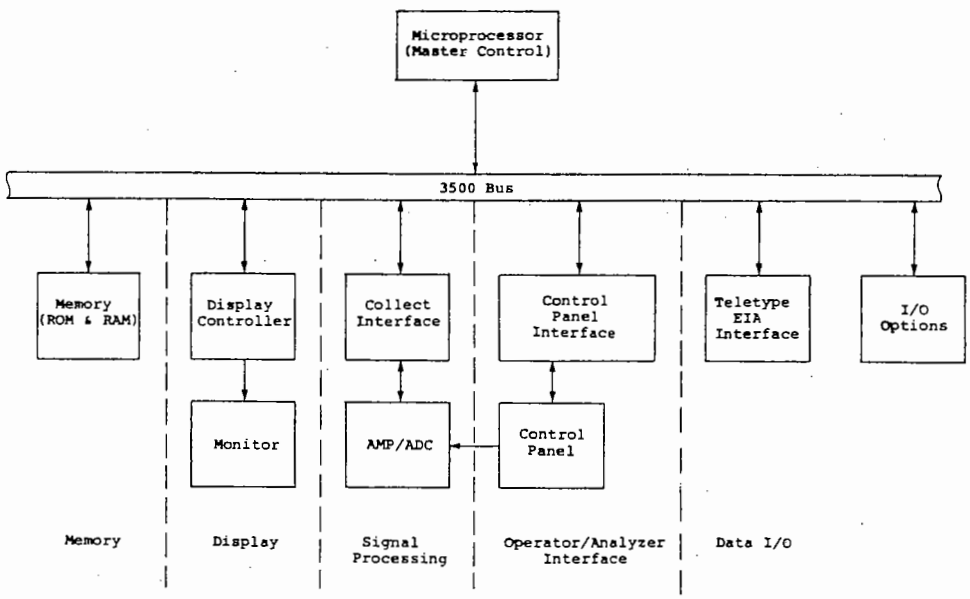

Figure 1.1
Series 35 PLUS Block Diagram

The Series 35 PLUS is offered with data memory of 2048, 4096 or 8192 channels. Memory storage in RAM can take place in the full memory, either half of the memory or any quarter of the memory as selected by the operator. Data storage may be either in the Pulse Height Analysis (PHA) mode, the Sampled Voltage Analysis (SVA) mode, or the Multichannel Scaling (MCS) mode. For both PHA and MCS, the data may be added to or subtracted from the memory.

The display section of the Series 35 PLUS directs the data in the memory to the large screen display and organizes it in readily understood format. The operator is supplied with a clear picture of the spectral data in memory and with appropriate information in alphanumeric form as an aid in interpreting the data displayed.

The signal processing section includes a preamplifier/amplifier that may be configured by the operator to accept either charge-sensitive input signals or voltage-sensitive input signals, depending on the type of detector to be used. The signals are passed to an Analog-to-Digital Converter (ADC), which converts the input linear signals to digital form and routes them to the appropriate memory location for storage and subsequent display, analysis and readout.

The operator/MCA interface allows the operator to direct the tasks of the MCA by means of the settings of the control switches and pushbutton keys on the front panel. The operator's instructions are routed through the keyboard interface to the RAM section of the memory by way of the microprocessor and the 3500 bus.

The input/output (I/O) section controls the data flow between the RAM section of the memory and the various peripheral devices. As a standard feature, this section includes the I/O interfacing needed to handle current-loop (Teletype*) and either EIA RS232 devices or the Canberra Model 5421M Cassette Recorder.

Provision is made for the operator to read prerecorded data into the memory as well as reading data out of the memory in the operator's choice of: full, half or quarter memory; any Regions of Interest, as specified by the operator.

By dividing the MCA's full range of operating features and analysis functions between several sections controlled by a high-speed microprocessor, the Series 35 PLUS has been made into an instrument that is well suited to both basic and advanced nuclear analysis needs.

1.2 APPLICATIONS

From a data acquisition point of view, all Series 35 PLUS Multichannel Analyzer applications can be placed into one of two categories: Pulse Height Analysis (PHA) or Multichannel Scaling (MCS). These two analysis modes and their applications are discussed in the following sections.

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1.3 PULSE HEIGHT ANALYSIS

In the PHA operating mode, a train of pulses, such as those from a radiation detector, are applied to the input of the Series 35 PLUS. These pulses have amplitudes (heights) which are proportional to the energies of the incident radiation that was absorbed by the detector. By counting the number of occurrences of pulses of each height and forming a histogram, the Series 35 PLUS records the radiation energy spectrum as seen by the detector.

A better term for Pulse Height Analysis would be Pulse Height Distribution Analysis, because the input pulses are sorted by voltage amplitude to yield a histogram representing frequency of occurrence versus pulse height. A pictorial representation of this process can be seen in figures 1.2 and 1.3.

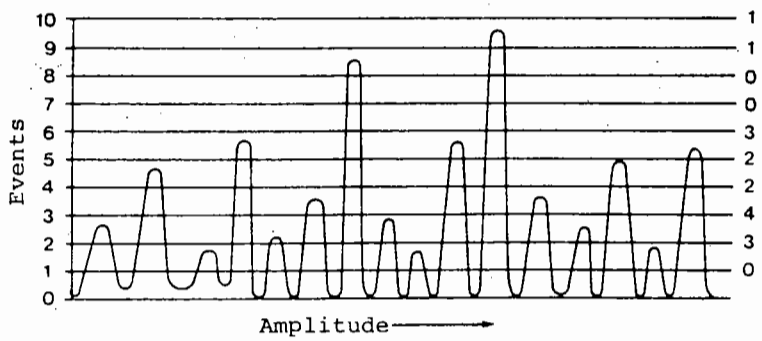


Figure 1.2
Input Voltage Pulses

Figure 1.2 depicts a series of voltage pulses as they might appear at the input to the Series 35 PLUS. The vertical axis has been divided into ten equally spaced intervals, each representing one volt of pulse height. The number of pulses falling into each of the intervals is tabulated at the right of the figure.

This same data is then shown in histogram form in figure 1.3, where the horizontal axis divisions correspond to the voltage divisions on the original signal. It is this type of pulse height distribution analysis that is performed by the Series 35 MCA during PHA mode data acquisition.

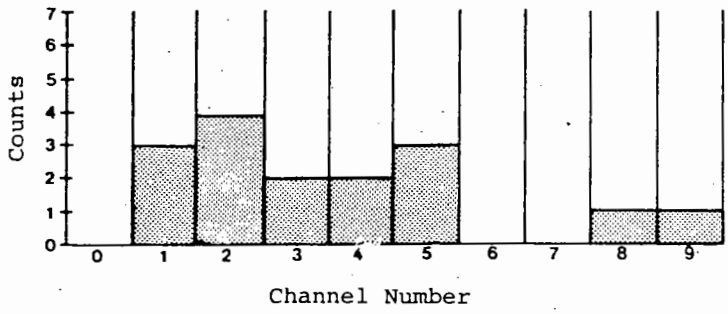


Figure 1.3
PHA Histogram

The primary application of PHA operation is in the quantification of the output signals from the class of radiation detectors whose output is a current or voltage pulse proportional in amplitude to the energy absorbed by the detector. Typical of such detectors are Scintillation detectors such as NaI (Tl), Semiconductor detectors such as Ge, HPGe, Si(Li), and Gas Proportional detectors.

A common characteristic of all these detectors is that each current or voltage pulse produced by the detector corresponds to the energy deposited by an individual photon or particle. Since the nuclear or atomic decay which generates the incident radiation is a randomly occurring process, the pulse train from the detector to the Series 35 PLUS is a time-random mixture of pulses of all possible amplitudes.

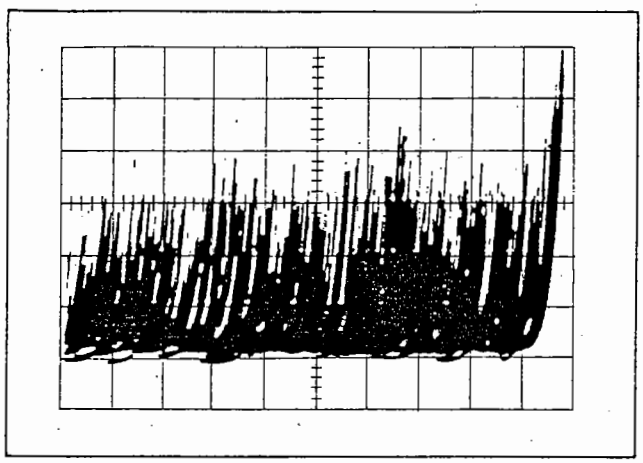


Figure 1.4
Voltage Train Output
from a Ge detector

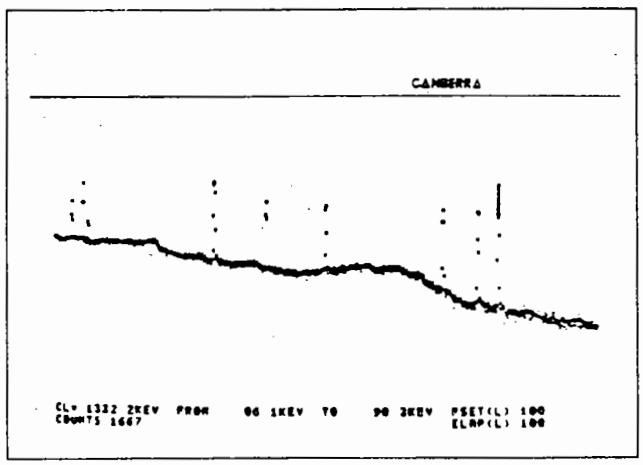


Figure 1.5
Resultant PHA
Histogram

The job of the Series 35 PLUS, in PHA operation, is to sort this pulse train by amplitude and store the resultant spectrum. This can be seen graphically in figures 1.4 and 1.5, where both the detector output and PHA histogram for a mixed gamma source are shown.

The 1024 channel histogram shown in figure 1.5 is directly analogous to the ten channel histogram in figure 1.3 but is of far greater resolution. That is, the input pulses have been sorted into 1024 discrete amplitude levels rather than just ten levels. Each point in the figure 1.5 display represents the number of counts accumulated in one particular channel; it is still a pulse height distribution histogram.

From an analytical point of view, a PHA distribution histogram (spectrum) can provide both qualitative and quantitative results. Since channel number corresponds to input voltage, and input voltage corresponds to the energy of the radiation striking the detector, the energy of any peak in the spectrum can be easily determined; and from the energy (or energies) present one can determine the source.

The spectrum can also yield quantitative data. Since all measurements of radiation intensity are based upon the number of events per unit time, one need only divide the number of occurrences of a given energy by the total acquisition time to get a measure of the activity present. This is, of course, an oversimplification, since there are many other physics-related factors that must also be considered. But conceptually, the principle of "counts divided by time" is valid.

1.4 True Time

Because of this, when operating in PHA mode, the Series 35 PLUS stores acquisition time along with the spectral data. Channels 0 and 1 of the Series 35 PLUS's memory are reserved for the time storage function. Channel 1 stores true (real) time.

1.5 Live Time

The time value stored in channel 0 is generated by a special circuit called a "live time clock", and the value accumulated is called the "live time". The need for this special time circuit can be seen by examining in closer detail the operation of the Series 35 PLUS PHA in relation to the input pulse train.

From a time standpoint, the input pulse train is totally random in nature. Therefore, since it does take the analog-to-digital converter (ADC) a finite amount of time to convert a pulse amplitude into a channel number, some pulses will arrive at the ADC only to discover that it is busy processing the previous pulse. The ADC is effectively "dead" and this datum (pulse) is lost.

1.6 DEAD TIME

Because of this "dead-time" phenomenon, a time correction circuit is required to compensate for the fact that the number of input pulses per unit time can vary considerably from the number of events stored per unit time.

This time correction circuit, called the "live time clock", extends the total elapsed counting time to compensate for the percentage of time that the ADC is "busy". This circuitry can be seen in operation via the Percent Dead Time bar-graph at the top of the Series 35 PLUS's display.

For PHA operation, the primary goals are, therefore, the ability to measure the distribution of input pulse heights and to keep track of the system live counting time. The time function is automatically handled via the live time clock and requires no parametric input. However, the Series 35 PLUS does provide several methods for modifying the parameters of the pulse height distribution function.

1.7 ADC GAIN

One of the factors affecting the generation of a pulse height distribution histogram is the system resolution; that is, the number of discrete voltage levels--or channels--into which the input pulses will be sorted. In ADC terminology, this is called the ADC Conversion Gain. For example, our initial histogram (in figure 1.3) used ten separate one-volt levels for sorting; it had an ADC Gain of 10.

For most PHA operations, the intent is to analyze the input voltage over its entire 0 to 10 volt range. To do this with maximum resolution, the ADC Gain is set equal to the Memory Size. For a 4096 channel (4K) memory, this corresponds to an ADC Gain of 4096.

Alternatively, an ADC Gain of 2048 channels would allow two separate spectra to be stored in either half of the 4096 channel memory.

1.8 DIGITAL OFFSET

For situations requiring greater resolution, the Series 35 PLUS ADC provides an ADC Gain of up to 8192 channels. However, since a 4K memory provides only 4096 channels of storage, only a portion of the input voltage range can be examined at one time using the 8192 channel ADC resolution.

If one were interested only in the first five volts of the zero to ten volt input range, the experiment's setup would be quite straightforward, as shown in figure 1.6. Pulses below the five volt (channel 4096) level are converted and stored; those above are ignored.

But what if the objective is to analyze those pulses in the five to ten volt range: how can this be accomplished? It is in this situation where the value of ADC Offset can be seen.

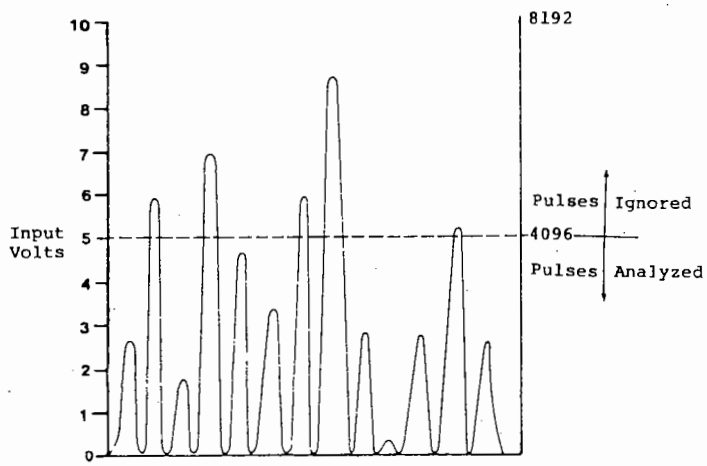


Figure 1.6
Effect of 8K Gain
and 4K Memory

Up to this point, it has been assumed that ADC channel numbers and memory channel numbers are the same. In reality they are independent, and it is the ADC Offset control which establishes their relationship.

When the ADC and memory channel numbers are the same, the ADC Offset is said to be zero. This relationship can be shifted linearly via the ADC Offset control.

For example, to analyze the upper five to ten volt range of the input using a 8192 channel ADC Gain and a 4096 channel memory, what is needed is to "shift" the zero channel of the memory to correspond to channel 4096 of the ADC. In other words, an ADC Offset of 4096 channels is required.

The Series 35 PLUS includes 32 different ADC Offset settings to allow the selection of the optimum value for any given situation.

1.9 MULTICHANNEL SCALING

MCS analysis yields a histogram representing number of events (radiation intensity) versus time. Just as in PHA, the input signal is a train of pulses, each representing a single event. However, MCS analysis does not concern itself with the amplitude of these pulses; the data stored is simply the number of individual pulses which were received in a given period of time.

As pulses are detected at the input of the Series 35 PLUS, MCS mode operation counts them one-by-one into the current memory channel for a predetermined period of time. At the end of this time period, which is called the dwell time, the MCS time base advances to the next memory channel address. Pulses are now counted into this channel for the dwell time period. Each memory channel is thus sequentially selected as a function of time.

1.10 MCS HISTOGRAM

This operation can be seen in a simplified form in figures 1.7 and 1.8. The input pulse train in 1.7 would generate the histogram shown in 1.8. Note that an MCS analysis produces an integral histogram; each channel represents the summation of all counts within the given time period and not the instantaneous count rate.

MCS analysis finds use in several applications involving the study of the distribution of events as a function of time. One such application is the study of nuclear decay; the resultant MCS histogram represents the exponential decay curve.

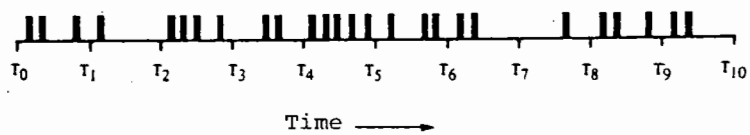


Figure 1.7
MCS Input
Pulse Train

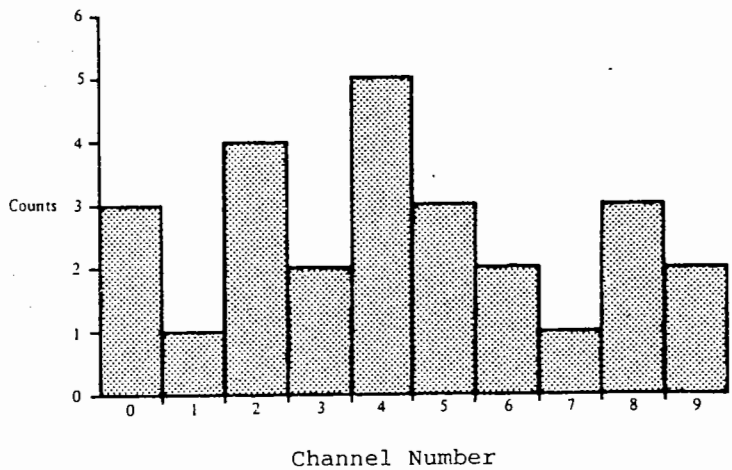


Figure 1.8
MCS Histogram

1.11 MÖSSBAUER SPECTROMETRY

Many other applications--such as Mössbauer spectrometry--involve the synchronization of the MCS scan to an external device. In this case, the time axis really relates to an external device position or condition, such as source velocity in the case of Mössbauer work.

1.12 DWELL TIME

For all applications an appropriate dwell time must be selected prior to the analysis. Several factors can influence this choice.

1. Desired time for the entire scan.
2. Number of channels to be used for data storage.
3. Desired counting statistics (number of counts per channel).
4. Operating rate of an external device.

In many cases, several of these criteria may be incompatible. For example, the sweep rate of a Mössbauer spectrometer may be too rapid to allow collection of adequate statistics in a single data acquisition scan. For these situations the Series 35 PLUS provides for multiple MCS cycles, which allows recurring MCS acquisition sweeps.

Depending upon the external device being used, it may be necessary to synchronize these recurring sweeps to the mechanical motion. The standard External Control/Mössbauer Wiring provides this capability.

SECTION 2
BASIC SERIES 35 PLUS OPERATION

This section describes the operation of the Series 35 PLUS, its data collection modes, and its basic dialogue rules.

2.1 POWER ON

Power is applied to the Series 35 PLUS with the ac power switch on the Analyzer's rear panel. Before applying power, check the voltage selection card inside the fuse compartment on the rear panel. This is easily done by moving the plastic fuse shield to the left and looking directly under the fuse; the operating voltage will be visible. To change the operating voltage, refer to Appendix A.1.

The Analyzer will be set for either 50 Hz or 60 Hz operation. To change the line frequency, refer to Appendix A.2.

The intensity of the display is controlled by the INTENSITY potentiometer located to the right of the display screen. A few seconds after power on, the display will appear and will look as shown in figure 2.1. The time and date shown are the clock's last readout when the power was turned off.

Note: In an Analyzer with a Model 3571, 3572, or 3573 interface, the display of figure 2.1 will not be seen at power on if the rear panel control switch is in the REMOTE position.

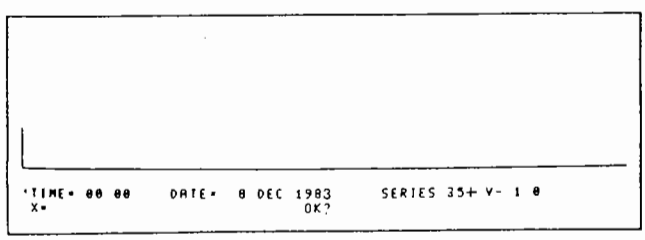


Figure 2.1
Initial Display

Note that the LED indicator for PHA+ on the Control Panel is illuminated. The Analyzer's default state assumes that the most common operating mode will be used; changing these modes is done by pressing a pushbutton for another mode. See section 4 for examples.

The usual first step after power is applied is the setting of the clock and the calendar to current values. The procedure for entering new values is:

1. Using the numeric keypad, enter the correct time in the form Hours.Minutes on a 24-hour basis. Note that the value is first entered in the X Register.

2. If an error is made in the entry, the CLR (clear) key on the keypad can be used to erase the value of X. A new value may then be entered in the X Register.

3. Press STORE on the keypad to transfer the entry from the X Register to the TIME variable.

4. Press NO to move the * to DATE and enter the new value for the date in the form DD.MM.YY and press STORE. Note: The year must be entered using the year's last two digits only. That is, 1984 is entered as 84.

5. Press YES (in answer to the question OK?) to have the new values accepted. The system's normal display will appear.

Note that the clock does not run when ac power is off. When ac power is restored, the clock will show its last reading as of power off time.

2.2 SYSTEM RESET

Associated with the INDEX and HOME keys is the System Reset command. The command is issued by simultaneously pressing these two keys.

Issuing a System Reset command aborts any operation in progress but does not alter any time or data information nor does it alter any operator-set parameters.

System Reset does not normally need to be used to abort an operation because most operations can be terminated simply by turning the function off.

Performing System Reset causes the display to revert to the initial power-on display seen in figure 2.1. It can be used to check the status of the system time and date clock and the system's firmware version. Answering YES to the question OK? will return the system to the normal display.

Note that System Reset causes the system to return to the PHA+ mode from any other data acquisition mode previously selected.

2.3 BASIC DIALOGUE PROCEDURES

The brief process of entering the current time and date, described in section 2.1, illustrates many of the basic dialogue "rules" common to all Series 35 PLUS operations. As the remainder of the manual is read, many additional examples will be seen. The following is a summary of those rules which are, in general, applicable to any dialogue sequence.

1. If a dialogue sequence is capable of accepting a numeric parameter, the X Register (X=) will be displayed on the lower left portion of the CRT.

2. During the entry of a numeric parameter, it is displayed as it is typed in the X Register. Errors may be corrected by pressing CLR and re-entering the value.

3. Touching STORE causes the entry in X to be evaluated and transferred to the parameter field being modified.

4. A numeric entry, up to 16 displayed characters, can be entered as an arithmetic operation. For instance, 5120 can be entered as X = 4096 + 1024. This entry will be evaluated and stored as 5120 when the STORE key is pressed.

5. The parameter field currently selected for modification is the one adjacent to the blinking *. To select a different parameter for modification, the blinking * must be moved to the desired parameter field.

6. When several choices are listed on a line, touching NO moves the blinking * to the next parameter on the line.

7. When the question NEXT? is displayed, pressing YES will mean "what is displayed is acceptable; go on to the next step." When the question OK? appears, YES will mean "I agree, end the dialogue."

8. If a dialogue procedure is aborted (by turning off the function rather than answering all questions), all original values are maintained as if the function was never started.

9. An illegal entry will generate an error message. To proceed, touch CLR on the numeric keypad and enter the correct value.

10. Under some conditions, a numeric display may show a series of "greater than" signs (>>>>). This indicates that the number is too large for the display field but will be correctly stored in memory.

The Series 35 PLUS also offers an additional operating characteristic that most users will find very beneficial after some "hands on" experience is gained: Function Type-ahead. That is, as keys are pushed, the code for each is stored in list (on a First In, First Out basis) and then retrieved in sequence for execution.

This allows an operator who is familiar with a procedure to quickly touch all needed keys, in the correct sequence, without waiting for the displayed dialogue to "catch up".

2.4 LED INDICATORS

Many of the front panel keys have a built-in light-emitting diode (LED) indicator to show the status of the associated function.

When any key is pressed, the function is enabled, and the LED, if there is one, is illuminated to show the status of the function. Pressing the key a second time will disable the function, turn off the LED, and abort any process that was initiated when the function was enabled.

Note that any prerequisites must be fulfilled before some of the functions can be enabled. For example, OVLAP cannot be enabled unless the MEMORY switch is in a position other than 1/1.

2.5 SIGNAL CONNECTORS

There are three BNC-type signal connectors at the upper left corner of the rear panel (figure 2.2). Two of these, labeled ADC IN and AMP IN, are analog signal inputs. The other connector, labeled GATE IN, accepts logic signals to condition the ADC to either accept or reject analog signals for conversion. See section 2.6 for information concerning use of the GATE input.

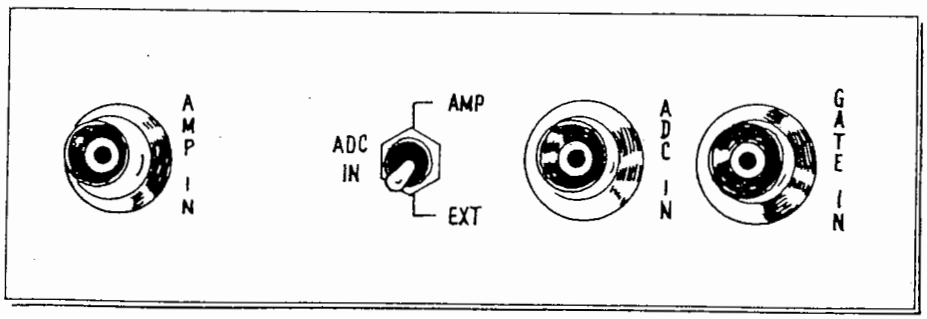


Figure 2.2
Signal Connectors

The AMPlifier INput can route signals from an external preamplifier to the internal amplifier or from a detector to the internal preamplifier (See section 2.7). The ADC INput accepts 0 to 10 V signals from an external amplifier which can then be processed by the ADC.

The adjacent ADC IN switch must be in the correct position for the input connector used. The AMPlifier position allows signals from the internal amplifier to be routed to the ADC; the EXTernal position connects the ADC INput connector directly to the ADC, bypassing the internal amplifier.

Care should be taken to keep the signal cables away from the display because it is possible for the display to induce noise on the input lines.

2.6 GATE

The GATE function allows the operator to enable or disable the ADC for acceptance and conversion of linear signals at its input. Depending on the criteria for the experiment in progress, the operator may use the GATE input in the factory-set coincidence mode or may change the function to the anticoincidence mode by moving a jumper on the ADC board (see Appendix A.3).

In order for the linear input signal to be considered by the ADC, it must be coincident in time with the GATE input signal.

In the Coincidence mode:

1. A low logic level (0 to 0.8 V) at the GATE connector will disable the ADC. It will neither accept nor process any linear signals while the GATE is low.

2. A high logic level (2.5 to 5.5 V) at the GATE connector will enable the ADC. It will accept and convert all linear signals received while the GATE input is high.

3. If the GATE input is left open (unconnected), the ADC will act as if the GATE Input is high and will accept and convert all linear signals received.

In the Anticoincidence mode, the logic is reversed. That is, a low logic level will enable the ADC and a high level (or an open input) will disable the ADC.

2.7 INPUT MODE

The Series 35 PLUS is factory-set to accept voltage pulses from an external preamplifier. These inputs signals are routed from the AMP IN connector to the internal amplifier.

The Analyzer can accept charge inputs directly from a detector, as in the charge-sensitive setup in section 3.1, by moving a jumper on the ADC Board (see Appendix A.3). Moving the jumper will route the AMP IN signals to the internal preamplifier before they are passed to the amplifier.

2.8 POSITIVE/NEGATIVE INPUTS

In the Voltage sensitive input mode (only), the Analyzer is factory-set for Positive-going input signals. See Appendix A.3 for instructions on accepting negative-going signals.

2.9 SAMPLED VOLTAGE ANALYSIS

In the Sampled Voltage Analysis (SVA) mode, analog voltages (dc or slowly changing ac voltages) can be sampled by the ADC, resulting in an amplitude distribution curve. The input signal must be a 0 to +10 volt signal and must fall between the settings of the LLD and ULD controls to be considered.

The GATE input is used as the sampling signal, which must be coincident with the voltage to be sampled.

To use the Analyzer in the SVA mode, the factory-set PHA jumper on the ADC board must be changed to the SVA position. See Appendix A.3. To return the Analyzer to the PHA mode, the jumper must be restored to the PHA position.

2.10 DEAD TIME

Any signal that is present at the input during the time that the ADC is processing a previous signal is ignored by the ADC. This is because the ADC is busy converting that previous signal and cannot accept another input until finished with the first. This busy time is referred to as the Dead Time.

The Dead Time is shown on the Series 35 PLUS's display as a bar graph, as in figure 2.3. It is displayed only in the PHA COLLECT mode.

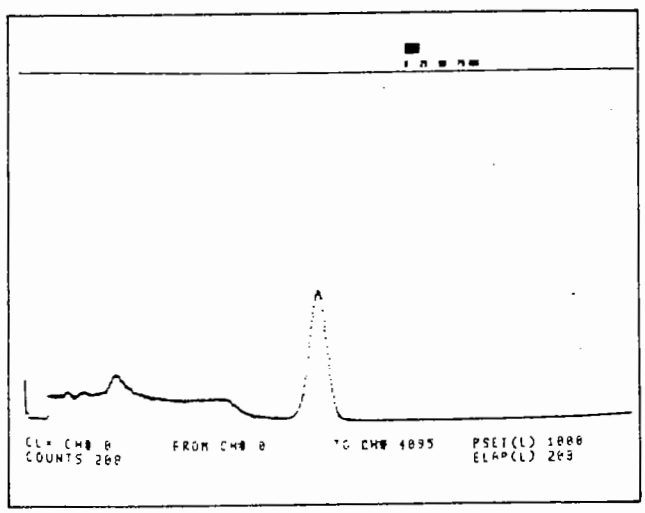


Figure 2.3
Typical Spectral
Display

SECTION 3
USING PHA AND MCS

This section will outline three experimental setups using the Series 35 PLUS and either a charge-sensitive input (from a scintillation detector, such as Canberra's Model 802 series) or a voltage-sensitive input (from any other type of detector).

See Appendix A.3 for instructions on changing from one type of input to the other. If a scintillation detector is connected to an external preamplifier the preamp's output can be connected to the Series 35 PLUS as a voltage sensitive input.

3.1 SETUPS

For a charge sensitive input, the following equipment, or equivalent, will be required:

- Series 35 PLUS Analyzer
- Model 3100-01 or Model 4261 High Voltage Power Supply (HVPS)
- Model 802 series Scintillation Detector
- Model 2007 Photomultiplier Tube Base
- Cables for interconnection as shown in figure 3.1

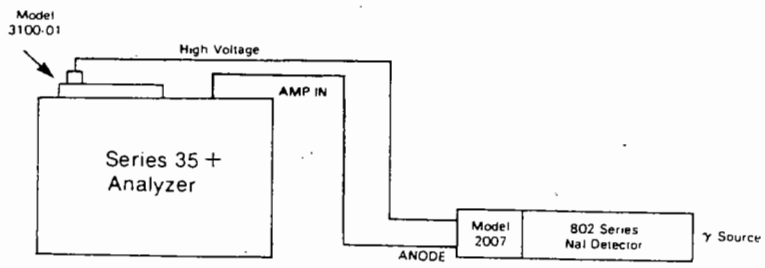


Figure 3.1
Charge Sensitive
System Setup

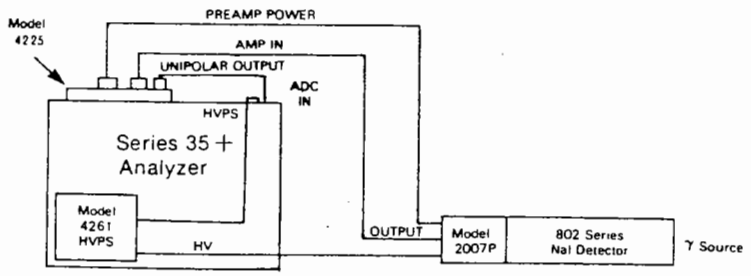


Figure 3.2
Voltage Sensitive
(NaI) System Setup

For a voltage sensitive input, the following equipment, or equivalent, will be required:

- Series 35 PLUS Analyzer
- Model 4261 High Voltage Power Supply (HVPS)
- Model 4225 Spectroscopy Amplifier. Note: NaI detectors can use the internal amplifier
- A Ge detector with a Model 2001 Preamplifier or a Model 802 Detector with a Model 2007P Preamplifier
- Cables for interconnection as shown in figure 3.2 or figure 3.3.

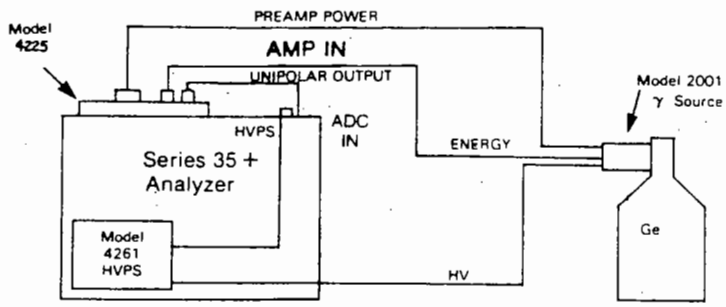


Figure 3.3
Voltage Sensitive
(Ge) System Setup

3.2 PHA DATA ACQUISITION

Initial Control Panel Settings:

ADC IN SWITCH	EXT for figures 3.2 and 3.3 AMP for figure 3.1
VERTICAL RANGE	1K or LOG
MEMORY	1/1
ADC GAIN	2048 (for Model 3501)4096 (for Model 3502) 8192 (for Model 3503)
ADC OFFSET	None: all switches down.
SCA LLD	0.20
SCA ULD	Fully clockwise
MODE	PHA+ (default state).

1. Turn on the Series 35 PLUS with the ac power switch, set time and date if desired, and press YES.

2. Turn on the HVPS with its separate switch.

3. Set the HVPS to the correct operating voltage for the detector being used.

4. Place a radioactive source near the face of the detector.

5. Press COLLECT to start data acquisition. Note that the LED indicator is illuminated in the COLLECT pushbutton, showing that acquisition is in progress. Note the Dead Time meter displayed at the top of the screen.

6. Adjust the AMPLIFIER GAIN so that the spectrum (data being displayed) is positioned conveniently on the screen.

7. Pressing CLEAR DATA repeatedly while adjusting the AMPLIFIER GAIN will aid in positioning the spectrum.

8. Allow the data to accumulate for a few minutes.

9. Press COLLECT again to stop acquisition. Note that the LED indicator is no longer illuminated.

3.3 DATA MANIPULATION

To see the effects of some of the front panel functions:

1. Change the MEMORY switch to 1/4.

2. Press XFER. The Analyzer displays two quarters with the upper data offset by 20% above the lower data. The dialogue asks if the operator wants to transfer Q#3 to Q#1 (memory quarter number three to memory quarter number one).

3. Press YES to enable the transfer. Note that the upper data trace is no longer displayed and the data has been copied into the memory section being viewed (Q#1).

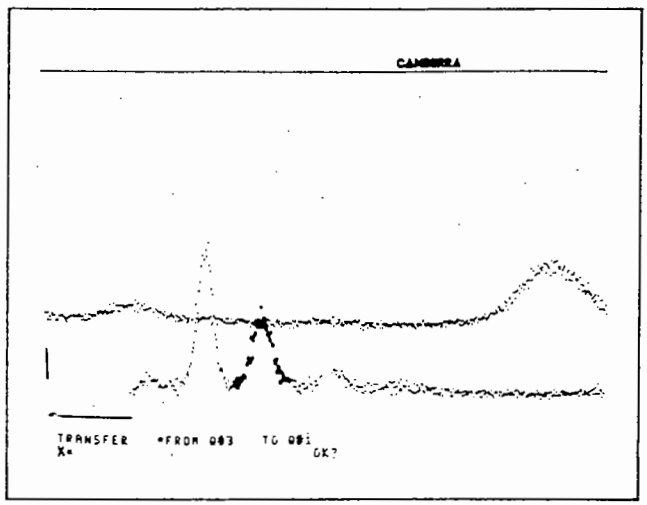


Figure 3.4
XFER Display

4. The cursor is moved by turning the Variscan control knob (SCAN) below the display. Turning the knob clockwise moves the cursor to the right; turning the knob counter-clockwise moves it to the left.

5. Move the cursor to the left side of a spectral peak, then press ENTER ROI. SCAN the cursor to the right side of the peak. Note that the peak's data points are intensified as the cursor moves through them.

6. Stop scanning and press ENTER ROI once more to disable the function. A Region of Interest has now been entered around the peak.

7. Repeat steps 5 and 6 for several more peaks.

8. Press INDEX and watch the cursor jump from the beginning of one ROI to the beginning of each succeeding ROI in turn. Note that the cursor will index from the last ROI in the spectrum to the first ROI.

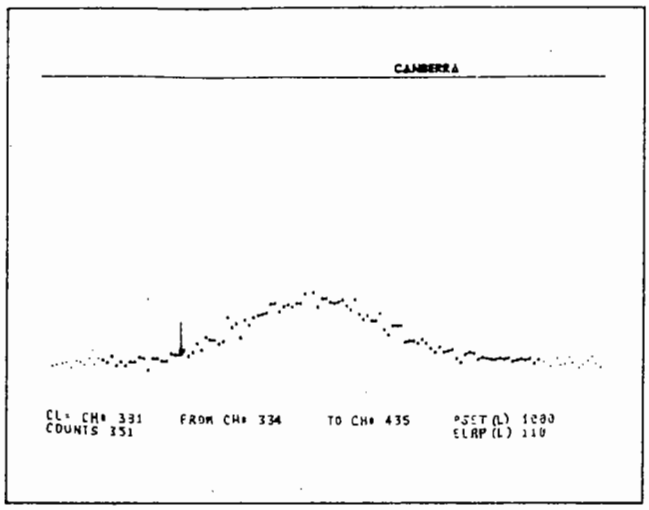


Figure 3.5
WINDOW Display

9. Press WINDOW to see the display change to include only 128 channels.

10. Press ROLL and then SCAN the cursor to the right. Note that the cursor stays at the same point in the display and the data appears to move to the left as the 128-channel Window is scanned to the right through the spectrum.

11. Press WINDOW again to disable the function. Note that the ROLL function is disabled simultaneously.

12. Press INDEX to move the cursor to an ROI.

13. Press AREA/INTEG and note that the area's histogram bars are displayed. The value of the net area is shown at the bottom of the screen, as is the value of the ROI's integral. (The Glossary defines these terms.) Disable AREA/INTEG.

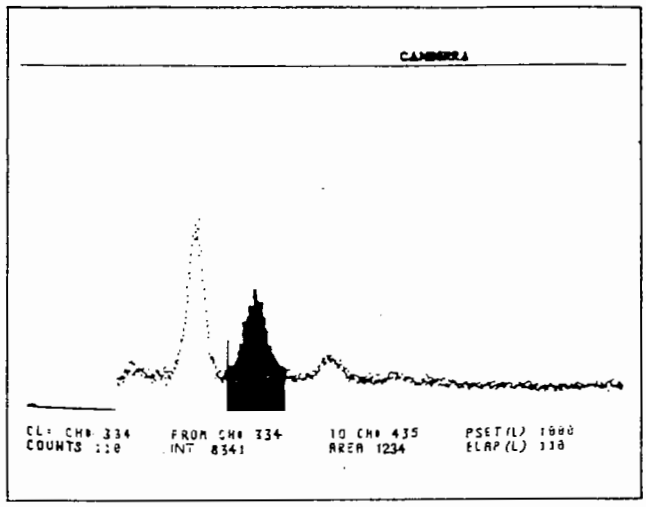


Figure 3.6
AREA/INT Display

14. The data displayed in Q#1 can be read out to a peripheral device by using the READ OUT function. See section 5, Input/Output, for instructions.

15. Press HOME. Note that the cursor has returned to channel 0, the first channel of the displayed segment.

16. Press CLEAR TIME. Look at the counts displayed for channel 0 (CL counts) and the ELAP (L) on the lower part of the display. Both should now read 0 (time has been cleared from memory). No data channels are affected by this function.

17. Press CLEAR DATA and note that all data has been cleared from memory. This function clears only the displayed section of memory; other sections are not affected. If CLEAR TIME had not been performed in the last step, pressing CLEAR DATA would have reset the two time channels, as well as all of the displayed data channels, to zero.

3.4 MCSR DATA ACQUISITION

To see the effect of MCSR operation, use the same setup and control settings as for the preceding PHA experiment.

1. If there are data in the memory, press CLEAR DATA.
2. With the sample near the face of the detector, press COLLECT.
3. Increase the LLD control setting until no pulse storage takes place below the energy of interest, such as one or more of the peaks. Repeatedly pressing CLEAR DATA while increasing the LLD control will aid in finding the desired setting.
4. Lock the LLD control, press COLLECT to stop acquisition and press CLEAR DATA to clear the memory.
5. The ULD control can be decreased in the same manner if data acquisition is not wanted above a specific energy level.
6. Press MCSR to change the analyzer to the MCSR+ mode.
7. Press COLLECT and observe the type of data displayed as a result of this different type of acquisition. Figure 3.7 shows a typical MCSR spectrum.
8. Press COLLECT to stop the MCSR sweeps.

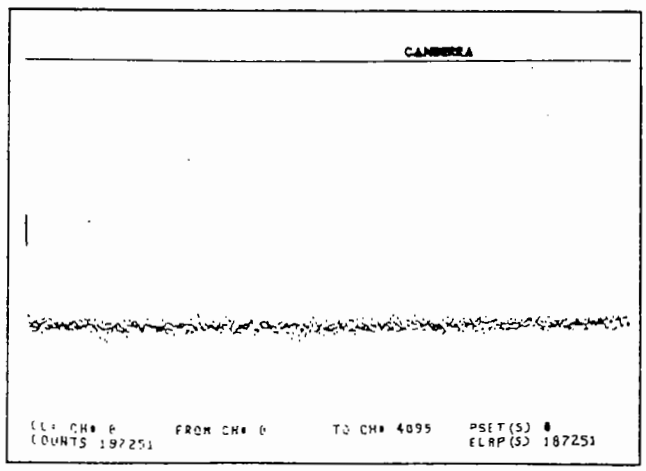


Figure 3.7
MCSR Display

SECTION 4
FRONT PANEL CONTROLS

All of the operator's controls for the Series 35 PLUS are located on the front panel, except for the Model 3573's Remote/Local switch, which is on the rear panel.

This section starts with a description of the keypad, then lists all of the other front panel controls alphabetically.

The controls for optional functions are listed separately. Section 7 covers the Model 3541 Define/Use/Ap-Pak option and section 8 covers the Models 3543 Isotope Analysis and 3544 X-ray Analysis options.

4.1 KEYPAD

The KEYPAD comprises ten digits, four arithmetic operators, a decimal point, and a CLR (clear) key. The Keypad enters parameters through the X Register and enters equations for the Define/ Use/Ap-Pak options.

The CLR key clears incorrect entries from the X register. It also ends an error condition and clears the error message from the display.

There are three associated keys to the left of the decimal point. YES and NO are used in parameter selection; refer to section 2.3. The STORE key moves the contents of the X register into memory.

4.2 ADC GAIN

This six-position rotary switch is used to establish the full scale resolution of the ADC, as discussed in the Introduction, section 1.3.1. The ADC Gain is commonly set to equal the number of channels of data acquisition memory; that is, a 4K memory (4096 channels) would commonly use an ADC GAIN of 4096.

For finer resolution over a narrower energy range, the ADC GAIN switch, in conjunction with the ADC OFFSET, can be used to display the energy range of interest.

4.3 ADC OFFSET

The ADC OFFSET establishes the relationship between memory channel zero and the ADC channel assignments. The effect of the Offset is to shift the spectrum by a selected number of channels.

For instance, if an ADC GAIN of 4096 is selected but only 1024 channels of memory are being used for acquisition, then the upper 75% of the spectrum will not be stored in the memory. If the upper 25% of the spectrum is to be stored in the memory, the ADC OFFSET will have to be changed from zero to some number that will shift the spectrum by the desired number of channels.

In this example, an Offset of 3072 (1024 + 2048), which equals the 4096 Gain less the 1024 memory size, will accomplish the shift by moving the zero channel of memory to ADC channel 3072. Converted pulses whose value is less than 3074, will be discarded and pulses which convert to 3074 will be stored in the first data channel of the memory (channel 2). Note that the offset switches are additive.

With ADC Gains of 512 or 256, the Offset indicated by the switches is divided by 2 or 4, respectively.

4.4 AMPLIFIER GAIN

The coarse and fine gain controls are provided to adjust the gain of the internal amplifier to the desired spectral energy range. Together they provide a gain range of 3 to 1170.

The coarse gain control is a five-position rotary switch. The fine gain control is a ten-turn precision potentiometer that multiples the setting of the coarse gain control by a variable factor which can be set as low as 0.3 or as high as 1.3.

The fine gain control is factory set to read 0.3 at its minimum setting so that its dial reads the variable factor directly, allowing the operator to set the amplifier's total gain with precision.

4.5 ANLYZ (Analyze)

The ANALYZE key can be used only when a Define/Use/Ap-Pak option is installed in the Series 35 PLUS.

Section 7 covers the option and the use of this key.

4.6 AREA/INTEG

This function will display the Area, its histogram bars, and the Integral of all of the data points in:

1. The current ROI (defined below) if ROIs are entered.

2. The entire memory segment displayed if no ROIs are entered. Histogram bars are not shown in this case.

The Integral is the total sum of all counts in the current ROI or in the displayed memory segment.

The Area is the Integral less the counts in the calculated background. The Area, Background, and Integral algorithms are given in Appendix D.

The current ROI is the ROI containing the cursor. If the cursor is not in an ROI, then the current ROI is the next ROI to the right of the cursor.

If the cursor is to the right of the right-most ROI, the calculation will be made for the left-most ROI in the spectrum.

4.7 CLR

The CLR key, located on the keypad, is used to clear incorrect entries from the X Register. It also aborts an error condition and clears the error message from the display.

4.8 CLEAR ALL

CLEAR ALL clears all ROIs from the displayed memory section.

In clearing any ROI, the data is not affected. Only the intensification is cleared from the memory.

4.9 CLEAR DATA

The K1 function is covered in section 7.

This function clears all channels in the chosen memory segment, including the time channels.

CLEAR DATA is usually used to reset the entire memory to zero before starting a new experiment or a new run of the current experiment.

4.10 CLEAR ONE

CLEAR ONE, if the cursor is not located within an ROI, clears the current ROI.

Current ROI is the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

If the cursor is located within an ROI, CLEAR ONE clears those channels within the ROI that are to the right of the cursor, as well as the channel containing the cursor.

In clearing any ROI, the data is not affected. Only the intensification is cleared from the memory.

4.11 CLEAR TIME

The "✓" function is covered in section 7.

This function clears the first two channels in the memory segment chosen by the MEMORY switch.

CLEAR TIME can be used to reset the two time channels to zero without erasing the existing data. The operator may wish to add or subtract new data using the same preset conditions as for the first data collection.

4.12 COLLECT

The COLLECT function starts or stops data acquisition in the mode already chosen by the operator. (The PHA+ mode, for instance.)

If MCSR acquisition is in progress, the firmware allows the operator to "STOP" or "ABORT" when terminating COLLECT. STOP = terminate at the end of the current sweep; ABORT = terminate immediately. ABORT is given as a choice only when the selected dwell time is equal to or greater than 2 ms.

When Collect is enabled or disabled, the analyzer reads the position of the Memory switch to start or stop data acquisition in that memory section. The Memory switch can then be changed in order to examine, manipulate or Read In/Read Out data in another section of memory.

4.13 ECAL

The "(" function is covered in section 7.

The Series 35 PLUS has the capability of calibrating the displayed spectrum in energy units. The cursor location and the limits of any entered ROIs will then be shown in those units instead of a channel address. Using this displayed energy information, an unknown radioisotope can be identified.

The Series 35 PLUS will accept up to 7 Energy Calibration equations, one for Full memory, one for each Half and one for each Quarter of memory.

In addition to the energy units EV, KEV and MEV, the Series 35 PLUS offers the time units MSEC, SEC and MIN for calibration of Multichannel Scaling. The procedure is the same as for the Energy Calibration.

The method uses a first order (straight line) calibration and is accomplished by answering the questions in the ECAL dialogue.

To calibrate a spectrum:

1. Press the front panel ECAL key to start the dialogue.

2. If this memory segment was previously calibrated, the equation will be displayed (see step 8). Press YES to accept the displayed equation.

3. Press NO to delete the old equation and write a new one. Advance the * to the desired calibration unit: EV, KEV, MEV, MSEC, SEC, or MIN. If the model 3544 X-ray Analysis option is installed, MEV will be replaced with KEV.3.

4. Press YES to advance to the parameter dialogue.

```
LOW:  CH#  0      0.0 KEV      HIGH:  CH#  0     0.0 KEV
X=                    OK?
```

5. Enter the LOW channel either as a channel number or by pressing STORE to enter the current cursor location.

6. Press NO to advance the *. Enter the Low energy and press STORE.

7. Press NO to advance the *. Enter the HIGH channel and energy as in steps 5 and 6.

8. Press YES to display the ECAL equation.

```
USE      ENERGY =  0.45656E01 * CH# + 0.106E00  KEV
                        OK?
```

9. Press YES once more to Use the equation and return to the Energy Calibrated spectral display.

Pressing ECAL again will disable the function. If an equation exists, pressing ECAL will show the equation for use. Press NO to delete the equation and write a new one.

4.14 ENTER ROI

The Series 35 PLUS has provision for entering Regions of Interest (ROIs) to mark significant peaks in the spectrum for later analysis and readout. To enter an ROI, simply position the cursor at one limit of a peak with the SCAN control, press ENTER ROI, and SCAN the cursor to the other limit of the peak.

Each data point that the cursor passes through while ENTER ROI is enabled will be intensified to indicate that the data is within the ROI. When the further limit of the desired ROI is reached, stop moving the cursor and press ENTER ROI once again to disable the function.

Any number of ROIs may be entered as long as they are separated by at least one channel. That is, ROIs may not overlap. Also see Section 4.25.4, Peak Search.

4.15 HOME

Pressing HOME moves the cursor to the left end of the display, either the memory section being displayed or the expanded display if WINDOW is enabled.

4.16 INDEX

The INDEX function is used to quickly move the cursor to the next ROI.

INDEX will move the cursor to the left limit of the next ROI to the right.

INDEX will "wrap around" the memory. That is, the cursor can be moved from last ROI on the display's right to the first ROI on the left simply by INDEXing.

If ROLL is enabled, INDEX will move the expanded data region to the next ROI and display its data.

4.17 INTENSITY

The INTENSITY control varies the brightness of the display. Turning the control clockwise will increase the intensity; counterclockwise decreases the intensity.

4.18 ISO ANLYZ

The Isotope Analysis key can be used when the Model 3543 Iso Analyze or Model 3544 X-ray Elemental Analysis option is installed in the Series 35 PLUS.

Section 8 covers the use of this key for the Models 3543 and 3544.

4.19 LLD (Lower Level Discriminator)

This ten-turn, locking potentiometer is used to establish the lower energy limit for input signals that are to be converted by the ADC. Input signals that are below the LLD setting in amplitude are not converted. If signals below the LLD setting are above the factory set threshold, those signals will add an increment of deadtime equal to the signal's width.

For MCSR operation, the LLD is usually set just below the energy of interest.

4.20 MCSR

The V1 function is covered in section 7.

The MCSR key selects the Multichannel Scaling, Recurring sweep made of data acquisition. The MCSR mode is described in section 1.4.

The Series 35 PLUS defaults to the PHA+ mode at power on or when the System Reset command is issued; refer to section 2.2.

When the MCSR key is first pressed, the additive (+) mode is selected. Pressing the key again enables the subtractive (-) mode.

In the additive (+) mode, all newly acquired data is added to the data already in memory.

In the subtractive (-) mode, all newly acquired data is subtracted from the data already in memory.

In the MCSR mode, channel 0 records the number of sweeps completed. Channel 1 is used as a dwell time register; refer to Dwell Time Coding in section 4.27.2. Channels 0 and 1 are always additive.

4.21 MEMORY

The MEMORY switch selects the section of memory to be:

- addressed by the ADC for data storage
- displayed by the CRT
- read out of or read into

The operator may select full memory, either half or any of the quarters.

- 1/1 refers to the full memory
- 1/2 refers to the first half of the memory
- 2/2 refers to the second half of the memory
- 1/4 refers to the first memory quarter
- 2/4 refers to the second quarter
- 3/4 refers to the third quarter
- 4/4 refers to the fourth quarter

Regardless of the memory segment chosen, the first two channels of the segment are used to register PHA Live and True time or MCS sweep count and Dwell Time code.

4.22 MIXER/ROUTER

The V2 function is covered in section 7.

If the Model 3531A Mixer/Router Wiring or Model 3523 Multi-ADC Interface is installed in the analyzer, pressing the M/R key will allow the operator to choose how many inputs the analyzer is to accept. The dialogue will read:

NO. INPUTS *2 4 8† 16†
OK?

---

†For the Model 3523, 8 and 16 are not shown

Choosing the number of inputs with the * will cause the Firmware to divide the full memory into the selected number of equal parts for separate data storage for each input.

To use the Series 35 PLUS with one input, the M/R key should not be used. The Mixer/Router should be disconnected from the system when a single input is desired.

Refer to the Mixer/Router's Operator's Manual or to the Model 3523 Multi-ADC Interface operating instructions, section 10.3, for more information.

4.23 NO

The NO key is used in parameter selection. Refer to section 2.3.

4.24 OVLAP (Overlap)

The OVLAP function is used to make a visual comparison between two spectra by superimposing a corresponding half or quarter memory over the currently displayed section of memory. Note that the function cannot be enabled if the MEMORY switch is in the 1/1 position.

The corresponding memory sections are:

Current Display	Overlapped Section
1/2	2/2
2/2	1/2
1/4	3/4
2/4	4/4
3/4	1/4
4/4	2/4

The operator can modify the first half of the OVLAP dialogue to display another overlapped section of corresponding size simply by entering the desired number by way of the X Register. The second half of the dialogue is always the memory section currently being displayed. The MEMORY switch must be changed to show the correct display before enabling the function.

The overlapped data are always displayed offset by 20% of the selected VERTICAL RANGE.

When the dialogue has been completed, pressing YES (in answer to OK?) will terminate the dialogue; the overlapped memory section will remain on the screen until the function is turned off by pressing OVLAP again.

After the Overlap dialogue has been completed, the MEMORY switch can be changed between halves or between quarters. This will allow other memory segments to be compared with the overlapped segment.

Note that if the MEMORY switch is changed outside of the original size memory segments, the function will turn itself off.

4.25 PEAK

The ")" function is covered in section 7.

The PEAK function can find valid peaks either manually, via the front panel key, or by way of a Task step. A valid peak is one which is found by the Peak Search algorithm using the selected sigma, or level of confidence.

4.25.1 Manual Peak

When manually started, the PEAK function searches the spectrum for valid radioisotope peaks, enters ROIs, and reports the Centroid and Full Width at Half Maximum (FWHM) for the current ROI.

Current ROI is the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

4.25.2 Task Peak

PEAK as a Task step searches for valid peaks and enters ROIs, but the Centroid and FWHM are not calculated. For a Task Peak Search to be successful, all previous ROIs must be cleared before the search starts.

4.25.3 Peak Sigma

In the PEAK function, sigma is used to determine if the peak is statistically significant compared to its background level. That is, if a small peak on a high background level is analyzed, a high sigma value will cause the routine to find that the peak is not significant.

In Peak Search, a peak that is not considered significant will not be marked with an ROI.

Press the PEAK key to see:

SIGMA: *0.41 1.65 3.27
OK?

Select SIGMA to correspond to the desired peak confidence level and press YES:

0.41 = 66% confidence
1.65 = 95% confidence
3.27 = 99% confidence

PEAK will now be disabled and this value of SIGMA will be retained by the Series 35 PLUS until a System Reset is performed.

4.25.4 Peak Search

After SIGMA has been selected, enabling PEAK again will result in:

1. If ROIs are present in the displayed memory, a blinking cursor will appear at the peak channel of the current ROI. The value of the ROI's Full Width Half Maximum (FWHM) and CENTroid will be shown. The INDEX key can be used to select a new ROI.

2. If no ROIs are present, a blinking "SEARCHING" message will appear and ROIs will be placed around any spectrum peaks found by the search.

   At the end of the peak search, the current ROI's Centroid and FWHM will be displayed. If no valid peak is found, the function will automatically be disabled.

   Current ROI is the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

The algorithms for FWHM, Centroid, and Peak Search are given in appendix D.

4.26 PHA

The PHA key selects the Pulse Height Analysis mode of data acquisition. The PHA mode is described in section 1.3.

The Series 35 PLUS defaults to PHA+ (additive mode) at power on or when the System Reset command is issued; refer to section 2.2.

Pressing the PHA key will change the mode to PHA- (subtractive mode).

In the additive (+) mode, all newly acquired data is added to the data already in memory.

In the subtractive (-) mode, all newly acquired data is subtracted from data already in memory.

In the PHA mode, channels 0 and 1 are used to record elapsed Live and True Time, respectively; refer to section 1.3.

Channels 0 and 1 are always additive.

4.27 PRESET

The K2 function is covered in section 7.

Each mode of data acquisition has its own default preset which can be changed as desired by the operator.

4.27.1 PHA Preset

The Series 35 PLUS provides five preset conditions for ending PHA data acquisition:

1. Live or true time.
2. Counts in a specific channel.
3. Total integral of a specific Region of Interest.
4. Total net Area of a specific Region of Interest.
5. Value of a USE equation with a Define/Use/Ap-Pak option. (Section 7.9 covers the Use Equation preset.)

Enabling PRESET brings up the following dialogue:

---

*TIME (L) TIME (T) COUNTS INT AREA USER VAL= nnn Units

X= OK?

The previous preset value (VAL= nnn Units) is displayed and may be changed through the X Register.

Using NO to advance the * allows the choice of True time, any of the three computational presets, or the user defined preset, which will bring up the question NEXT? in place of the question OK?

Counts

A response of YES (to NEXT?) changes the dialogue to allow the operator to enter, in the case of counts, the desired number of counts and the specific channel that the analyzer is to monitor for that count level.

When the * is at CHANNEL #, the current location of the cursor may be entered simply by pressing STORE.

Int/Area

If INT/AREA is chosen, the next line of dialogue will read

INT (or AREA) nnn COUNTS ROI FROM CH # n TO CH # n
X= OK?

Enter the number of counts and press NO to advance the * to ROI. Pressing STORE will enter the limits of the current ROI. When the * is moved to FROM or TO, the ROI limits may be entered manually or by pressing STORE, which will enter the current cursor address.

Current ROI is the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

It should be noted that, except in the case of Live Time, acquisition does not stop exactly at the preset parameter. This is because Series 35 PLUS's Firmware prevents fraction of a second errors in the keeping of Live Time. When the Analyzer reaches preset, collection will stop at the next tick of the Live Time clock.

A high Dead Time could cause a long real time to elapse before the next tick of the Live Time clock. In this case, Collect may be aborted by disconnecting the signal cable or by performing a System Reset (section 7.2).

4.27.2 MCSR Preset

If MCSR has been enabled, the PRESET dialogue will show:

```
DWELL (Nx10↑M USEC) N= 1 M= 2      SWEEPS = 0
X=                       OK?
```

The formula in parenthesis is read as "N" times 10 to the "M" power microseconds. The preset shown is set for 100 microseconds dwell time per channel.

The MCSR preset is defined by the following rules:

1. "N" can be set for 1 through 15.
2. When "M" is set to 9, the dwell will be expressed as "N" minutes.
3. When "M" is set to 10, the dwell will be expressed as "N" hours.
4. When "M" is set to 11, the dwell time will be set to "N" times 10 minutes.

5. When "M" is set to 15, the channel advance, and thus the dwell time per channel, will be under EXTernal control.
6. Setting the preset to EXTernal will cause the firmware to count "N" External pulses before executing a channel advance.

The number of sweeps may be preset for the required number through the X Register. If the default parameter of zero is retained, the analyzer will interpret this as infinity. That is, the analyzer will continue to sweep through the memory until stopped manually or remotely.

If MCSR acquisition is in progress, the firmware allows the operator to "STOP" or "ABORT" when terminating COLLECT. STOP = terminate at the end of the current sweep; ABORT = terminate immediately. ABORT is given as a choice only when the selected dwell time is equal to or greater than 2 ms.

NOTE: The number of sweeps performed may, under some conditions, exceed the preset slightly.

Dwell Time Coding

When MCSR Collect is started, the dwell time will be encoded and stored in channel one. If the number in channel one is divided by 16, the result will be the "N" factor. A remainder of 1 to 8 will be the "M" factor in microseconds; a remainder of 9 to 15 is explained in the next paragraph.

If the remainder is 9, M = minutes x 1.
If the remainder is 10, M = hours.
If the remainder is 11, M = minutes x 10.
If the remainder is 15, M = external pulses.

4.28 READ IN AND READ OUT

The "EEX" and "TL" functions are covered in section 7.

These keys control the input/output flow of data from or to a peripheral data storage device, such as a Teletype, a Cassette Tape or a Plotter. Their use is covered in detail in section 5.

4.29 ROLL

When enabled, ROLL allows the Window to be moved through the spectrum by means of the SCAN control. Scanning the Window will cause the data channels to appear to move in the opposite direction from the direction of scan, while the cursor remains in place.

Since this function is dependent on WINDOW, enabling the function automatically enables WINDOW if it is not already enabled. Similarly, disabling WINDOW will automatically disable ROLL.

4.30 SCAN

The VARISCAN control, below the center of the display, moves the cursor through the spectrum.

- Turn the VARISCAN control clockwise to move the cursor to the right.
- Turn the VARISCAN control counterclockwise to move the cursor to the left.
- Turn the VARISCAN control slowly to move the cursor through one channel at a time.
- Turn the VARISCAN control rapidly to move the cursor through a large number of channels.

Note: Turning the VARISCAN control generates a current proportional to the rate of turn. If you turn the control very slowly, the current won't be detected and the cursor won't move.

4.31 SMOOTH

Smoothing is used to decrease or eliminate random fluctuations in spectral data.

The function examines three channels at a time and averages the data in each channel with the data in the channel to either side. The Smoothing algorithm is listed in appendix D.

If WINDOW is enabled, only the expanded channels are smoothed. If ROIs are entered, only the current ROI is smoothed.

The current ROI is the ROI containing the cursor. If the cursor is not in an ROI, then the current ROI is the next ROI to the right of the cursor.

While the smooth operation is being performed a "BUSY" message will be displayed in the lower right corner of the display.

4.32 STORE

The STORE key moves the contents of the X Register into memory. Refer to section 2.3.3.

4.33 STRIP

The STRIP function allows the operator to subtract a factor-specified part of one spectrum, the reference, from another spectrum of the same size, the sample. The Strip algorithm is given in appendix D.

Before enabling the function, use the MEMORY switch to display the sample spectrum.

Press STRIP, which also enables OVLAP, to display the reference spectrum above the sample spectrum. The overlapped memory segment will be the one corresponding to the setting of the MEMORY switch as listed in section 4.24, OVLAP.

If the overlapped memory segment is not the desired segment, use the X Register to change the first part of the displayed dialogue.

```
STRIP *Q#1      FROM Q#3      F = 1.00
X=                            OK?
```

The factor (F) shown will be the last factor entered or the default parameter of 1.00. It can be changed by advancing the * by way of NO and entering another factor through the X Register. Leading and trailing zeros don't need to be entered.

The Factor's range is 0 through ± 327.67.

4.34 TASK

The Task key is used to select the LEARN/EXECUTE function of the Series 35 PLUS. Use of this function is explained in section 6.

4.35 ULD (Upper Level Descriminator)

This screwdriver-adjustable potentiometer controls the upper energy limit for pulses to be processed by the ADC. Input signals that are above the ULD setting in amplitude are not converted.

For MCS operation, the ULD is usually set just above the particular energy of interest.

4.36 VERTICAL RANGE

This eight position rotary switch selects the desired full-scale count value for the display, from 256 to 1048K (1 048 575) counts per channel, plus LOGarithmic display. The highest setting equals $2^{20}-1$ counts.

The switch is normally set so that the highest peak in the spectrum is no higher than the top of the display. If a channel accumulates more counts than can be displayed, the channel will "overflow". This is seen as a peak which appears to have its top cut off and is increasing in height again from the baseline. If a channel overflows the VERTICAL RANGE, increase the VERTICAL RANGE setting.

4.37 WINDOW

For a detailed visual analysis of the peaks within a spectrum, the Series 35 PLUS provides a variable horizontal expansion of the display.

Enabling WINDOW will cause the displayed data to change from the full display to an expanded portion of the display, 128 channels wide. The cursor will be located at the 49th channel of the expanded Window.

If the cursor is within 49 channels of the left end or within 79 channels of the right end of the normal display, it will remain in its original position.

INDEX will move the expanded window from the current ROI to the next ROI.

The current ROI is the ROI containing the cursor. If the cursor is not in an ROI, then the current ROI is the next ROI to the right of the cursor.

In order to examine peaks of interest that may fall outside of the Window, the Series 35 PLUS allows the size of the Window to be multiplied by a factor of two. Pressing the "X" key on the keypad will double the number of channels in the Window, expanded around the cursor. The cursor's location will not change: it will remain in the same channel and will still be at the 38% point of the multiplied Window.

Each time the "X" key is pressed, the Window size will be doubled again, up to a maximum of one-half of the selected normal memory region, but no more than 1024 channels.

To decrease the multiplied Window, press the "÷" key on the keypad. This will divide by two the number of channels in the Window, down to a minimum of 128 channels.

4.38 XFER (Transfer)

The XFER function allows the operator to copy data from one memory segment to another.

Energy Calibration equations are transferred with the data. ROIs are not transferred.

Enabling XFER simultaneously enables OVLAP and displays the corresponding memory segment, as listed in 4.24, OVERLAP.

```
TRANSFER  *FROM H#2 TO H#1
X=                   OK?
```

If the default parameters are acceptable, pressing YES will copy the data from the upper, overlapped, segment to the lower, current, segment.

The default parameters are alterable through the X Register to allow the overlapped memory segment to be changed to a segment other than the corresponding segment. The only restrictions are that the segment being transferred to must be chosen by the MEMORY switch and that the transfer can only take place between segments of the same size.

4.39 YES

The YES key is used in parameter selection. Refer to section 2.3.

4.40 ZERO

The analyzer is shipped with the ZERO control set for the memory size installed.

The ZERO control is a screwdriver-adjustable potentiometer which shifts the ADC zero relative to a zero energy (0 volts) input. This is done by shifting the spectrum by up to 5% of the ADC GAIN being used. It can be used like the ADC OFFSET to provide a fine control for positioning peaks.

The ZERO should be recalibrated each time the ADC GAIN is changed but is not critical. The result of not readjusting the ZERO will be a slight shift in the spectrum's peaks and slight change in linearity.

When performing experiments which require better linearity, channel zero of the Analyzer is usually made to correspond to zero energy input. Appendix C lists two methods for setting the ZERO control.

SECTION 5
INPUT/OUTPUT

The READ OUT and READ IN functions are used to store or retrieve data. This section covers the use of these two functions.

5.1 DATA READOUT

The READ OUT pushbutton allows the operator to transfer data from the Series 35 PLUS's memory to a peripheral recording device. When enabled, the last-used readout parameters are displayed with current tag number, time, date, and Data ID. For example:

```
DEV: EIA   MEM: ROI   MODE: ASCII    TAG: 2   (TIME AND DATE)
ID: SERIES 35+ V-1.0      OK?
```

Answering YES (to OK?) will start the readout using those parameters. Answering NO will allow the parameters to be changed:

```
DEV=  TTY  *EIA                  TAG = 0
X=                          OK?
```

Other device codes will appear in addition to the above listed codes if their I/O interfaces are present in the Analyzer:

- TTY Selects current-loop device readout.
- CAS Selects Cassette readout. Sets the baud rate (1200) and leader generation for the Model 5421M Cassette Recorder. Mutally exclusive with EIA.
- EIA Selects EIA (RS-232) device readout. Mutually exclusive with CAS.
- X-Y Selects Model 3551 X-Y Plotter.

LPT Selects Model 3552A Serial Printer.
PLT Selects Model 3552A Serial Plotter.
GRA Selects Model 3553 Graphics Plotter.
MT Selects Model 3554 Magnetic Tape.

The default state readout device is either EIA or CAS (see notes). By moving the *, the operator may choose to read data out to any other available peripheral device.

The last item in this dialogue allows the operator to set a Tag Number for identifying a particular readout; its use is not necessary to obtain a readout. The Tag Number will automatically be incremented by one with each readout.

NOTE 1

CAS may be replaced by EIA, depending on the position of an internal control switch. See Appendix A.5 for information on changing the switch position.

NOTE 2

Models 5107 (Teletype* Model 4320-AAK) and 5113 (Teletype Model ASR 43) connect to the EIA port (J101) using the supplied C1506 Cable. The dialogue must read EIA, not CAS.

With some I/O devices, pressing YES will start the readout. With others, answering YES to the question OK? will bring up the next line of the dialogue:

MEM+MODE	*ROI+ASCII	FULL+ASCII	ROI BRIEF	FULL+BINARY
		OK?		

MEMory plus MODE refers to the choices on the remainder of the line: memory choice and readout mode choice.

*Teletype is a registered trademark of Teletype Corp., Skokie, Ill.

The modes offered are different data transfer codes. Most peripheral devices can recognize only one mode; the instructions for each device will specify which mode is to be used.

MEM: FULL will read out all of the data in the memory segment selected by the MEMORY switch position.

ROI will read out the Live and True times and the data in all Regions of Interest in the selected segment of memory.

MODE: ASCII puts the read out data in a format suitable for a terminal. BINARY puts the read out data in a format suitable for the Model 5421™ Cassette Recorder.

ROI BRIEF will provide an ASCII readout of ROI summaries without the raw data.

If the wrong mode is chosen for the peripheral device being used, the data read out will be unintelligible.

5.2 DATA READIN

To read prerecorded data into memory or to enter a Data ID (section 5.6), press READIN to see:

DEV = TTY *EIA (see note in section 5.1)
OK?

Select the device and press YES to start the readin.

5.3 CASSETTE READOUT

The Model 5421M Cassette Recorder provides a convenient low-cost means of storing spectra collected with the Series 35 PLUS. This section describes the operating procedures for storing and retrieving (reading out and reading in) data using the Cassette Recorder. It will accept data in either the ASCII mode or the binary mode. The binary mode is normally used because ASCII characters use more tape space and take more time to transmit.

Model 5421M Cassette Recorder:

Connect the interface cable's three plugs to the recorder's EAR, MIC, and REM sockets.
Connect the other end of the cable to the Model 5421M's CASSETTE connector.
Connect the Cassette's line cord to a source of ac power.

Model 5421F Cassette Interface:

Connect the MCA connector to J101 (EIA) on the Series 35 PLUS's rear panel with the supplied cable.
Be sure the TERMINAL/CASSETTE switch is in the OUT position.

Recording Data

1. Put a blank cassette in the Recorder.
2. To rewind the cassette, press the Model 5421F's REMOTE button in and turn it clockwise to lock; press the Model 5421M's REWIND button.
3. Reset the recorder's counter to zero by pressing the button next to the counter.
4. Turn the 5421F's REMOTE button counter-clockwise to release it.
5. Press the RECORD button.
6. Press READ OUT on the Series 35 PLUS's front panel.
7. Select CAS and Press YES.
8. Select Full Memory and Binary Mode (FULL+BINARY).
9. Press YES again to start the readout.

Series 35, Series 35 PLUS, Series 40, Series 80, and Series 85 recorded data are mutually compatible and data from all of these MCAs can be read in to the Series 90.
Series 30 recorded data can be read in to any of these MCAs.

After the readout is finished, wait a few seconds for tape motion to stop. When the tape has stopped, record the number shown on the digital counter. This will be the spectrum identification number associated with the next spectrum recorded. To record another spectrum, repeat the procedures listed above, starting with step 4.

5.4 CASSETTE READIN

To read data into the Series 35 PLUS from a cassette tape, follow these instructions.

1. Insert the cassette containing the desired data into the Recorder.
2. Rewind the cassette to its beginning with the REV/REW button.
3. Reset the Recorder's digital counter to zero by pressing the button next to the counter's readout.
4. Using the CUE/FFWD button on the Recorder, search the tape until the desired spectrum ID number is displayed on the digital counter. If the number is overshot, use REV/REW to back up the tape as needed. Note that positioning of the tape is not critical: ±1 digit is adequate.
5. Press the PLAY button.
6. Press the READ IN button on the Series 35 PLUS's front panel.
7. Select CAS and press YES to start the read in.

Tag number, ID, and ECAL equation will be read in with the data.

5.5 TELETYPE I/O (TTY)

In addition to the EIA/Cassette interface, the Series 35 PLUS also includes a standard Teletype current-loop interface. For the Models 5107 and 5113, use the supplied C1506 cable to the EIA connector (J101) and refer to the Model 5107 or 5113 Operator's Manual for details of operation. To use the current loop (TTY) port, a Model C1406 cable is required.

Note that an ASCII-encoded paper tape is mutually compatible with the Series 35, Series 40, Series 80, and Series 85. A paper tape made by a Series 30 can be read into the Series 35 PLUS.

Connect the Teletype to J102 (TTY, the current loop port) on the Series 35 PLUS's rear panel. Apply ac power to the Teletype and move its mode switch to the LINE position.

1. Press READ OUT on the Series 35 PLUS's front panel.
2. Select TTY and press YES.
3. Select either FULL+ASCII or ROI+ASCII.
4. Press YES to start the readout.

The results of a FULL+ASCII hard copy readout are shown in figure 5.1. The results of a ROI+ASCII hard copy readout are shown in figure 5.2. The results of an energy calibrated ROI+ASCII hard copy readout are shown in figure 5.3.

TAG NO. = 1 FULL MEMORY READOUT PAGE 1
MEMORY= 1/2 LIVE TIME= 400 TRUE TIME= 473 3 APR 84 13:25

CHANNEL #	DATA							
0	400	473	158	128	148	148	146	127
8	149	144	131	151	148	133	149	135
16	165	163	151	124	155	167	159	153
24	153	149	135	134	154	130	160	156
32	121	148	149	149	141	141	137	145
40	149	157	157	140	159	168	119	129
48	140	127	152	153	133	147	145	135
56	142	131	125	151	143	147	148	125
64	123	149	160	153	141	149	116	161
72	154	121	125	137	152	148	126	143
80	142	146	150	163	136	155	167	142
88	153	140	151	141	158	144	131	128
96	132	141	134	135	117	155	139	156
104	135	130	147	146	160	145	130	135
112	136	149	137	138	162	127	144	139
120	152	147	138	158	142	103	158	159
128	133	123	142	130	135	145	139	138
136	166	148	153	126	134			154
144	142	150	142	147				
152	150	130	143					
160	135	143						
168	143	133						
176	148							
184								

Figure 5.1
Full Memory Readout

```
TAG NO. =        2          READOUT OF 2 ROIS                    PAGE    1
MEMORY= 1/2  LIVE TIME=     4000 TRUE TIME=     4080     3 APR 84  13:23

ROI#   1  FROM     162 CH#  TO     179 CH#
          INTEGRAL     31204       AREA     8299
          CENTROID  0.16922E03     FWHM  0.36774E01

ROI#   2  FROM     236 CH#  TO     252 CH#
          INTEGRAL     40229       AREA    17866
          CENTROID  0.2437E03      FWHM  0.39598E01
```

Figure 5.2
ROI Readout

```
TAG NO. =        2          READOUT OF 2 ROIS                    PAGE    2
MEMORY= 1/2  LIVE TIME=     4000 TRUE TIME=     4080     3 APR 84  13:23

CHANNEL#                              DATA
  162       1279     1281     1299     1383     1633     2189     2926     3335
  170       3054     2331     1692     1368     1260     1234     1230     1232
  178       1235     1243

  236       1317     1318     1314     1362
  244       5625     4646     3089
  252       1265
```

```
TAG NO  =        3          ECAL ROI READOUT                     PAGE    1
MEMORY= 1/2  LIVE TIME=     4000 TRUE TIME=     4080     3 APR 84  13:32

ENERGY(KEV )=   0 45664E00 * CH# +  0 10629E02

ROI#   1  FROM    65 3 KEV  TO    91.2 KEV
          INTEGRAL     26215       AREA     7511
          CENTROID  0 66099E02     FWHM  0 17296E01

ROI#   2  FROM   118 6 KEV  TO   125.9 KEV
          INTEGRAL     40229       AREA    17866
          CENTROID  0 12211E03     FWHM  0 18062E01
```

Figure 5.3
Energy Calibrated
ROI Readout

```
TAG NO  =        3          ECAL ROI READOUT                     PAGE    2
MEMORY= 1/2  LIVE TIME=     4000 TRUE TIME=     4080     3 APR 84  13:32

CHANNEL#                              DATA
  163       1281     1299     1383     1633     2189     2926     3335     3054
  171       2331     1692     1368     1260     1234     1230

  236       1317     1318     1314
  244       5625     4646
  252       1265
```

5.6 DATA ID

As an aid in identifying the data recorded in a given readout, the Series 35 PLUS provides a means of entering an alphanumeric identification (ID) label of up to 24 characters.

To enter an alphanumeric ID label with a current-loop device (TTY) or an EIA terminal:

1. Press READIN.
2. Choose TTY or EIA.
3. Press YES to activate the terminal keyboard.
4. On the terminal keyboard type:
   a. CTRL/B (press CTRL and the letter B).
   b. Any alphanumeric label of up to 24 characters
   c. CTRL/D (press CTRL and the letter D).
5. When the CTRL/D is received, Readin will terminate. Press READ OUT to display the label.

This ID label will be read out with all data from the Analyzer and read in with all data from an external recording device.

5.7 MODEL 3551 X-Y PLOTTER

The Model 3551 X-Y Plotter Interface is compatible with standard X-Y point plotters, such as the Hewlett-Packard 7041A (Canberra Model 5202A) or the HP7004B (former Canberra Model 5202). It will also support the Houston 2600CZ (former Canberra Model 5201).

If the interface is to be used with any other point plotter, refer to Section 5.7.2 for Specifications and Signals and to Appendix A.7 for interface board jumper locations and uses.

5.7.1 HP Plotter Operation

Set the Hewlett-Packard plotter's front panel switches to:

Null Detector	ON
Recorder	MUTE
Plot Rate	EXT

Refer to the plotter's operating manual for detailed operating instructions. Connect the Interface cable to P1 and P2 on the underside of the plotter's rear panel.

The Model 3551 Interface plots spectral data only; it generates a plot that corresponds to the spectral portion of the display. Therefore, the desired display should be set up before starting a plot readout.

1. If WINDOW is enabled, the plot will show the expanded section of the display only.
2. If OVLAP is enabled, the plot will show both traces as seen on the display.
3. Data in the section of memory being read out should not be changed during readout.
4. After readout has started, the MEMORY switch may be changed to display another section of memory without affecting the data being read out.
5. Data in another section of memory may be altered without affecting the data being read out.

Starting a Plot Readout

1. Press READ OUT on the Series 35 PLUS.
2. Select X-Y as the readout device.
3. Press YES to start the readout.

The tag word will not be read out by the plotter. A typical plot is shown in figure 5.4.

5.7.2 Specifications and Signals

Data can be recorded in either log or linear format in the line plot or point plot mode on X-Y or T-Y plotters.

A. Specifications

Signal Amplitude	0 to + 5 V
Resolution	1 part in 1024 (10 bits)
Output Impedance	≃ 93 ohms.
Integral Nonlinearity	<±0.1% of full scale per °C.
Zero-Drift	<±0.0 % of full scale per °C
Gain-Drift	<±0.02% of full scale per °C
Internal Rate Control (RV1)	Adjustable from 2 to >10 channels/sec. Factory set at 2 per second.
External Rate Control	Must exceed internally set rate. Maximum advance rate is >100 per sec.

B. Signals

J107 (or J108), 25-pin connector

Pin	Signal	Description
23	PLTX	0 to + 5 V analog signal.
2	XGND	Ground.
21	PLTY	0 to + 5 V analog signal.
4	YGND	Ground.
5	SEEK	Nominal 100 µsec output pulse when plot signals are changed; TTL compatible; positive true polarity is standard; internal jumper plug (D-E) inverts polarity.
6	CPC	Completed plot input from plotter; ac coupled; advances on negative going edge; minimum excursion = 4 V; rise time <0.5 µsec.
9	NABL	Plotter enable output; TTL compatible; negative true polarity is standard; internal jumper plug (B-A) inverts polarity.
14	GND	Ground.

5.7.3 Hewlett-Packard Plotter Cable Connections

The Hewlett-Packard 7041A Plotter uses a Canberra-supplied interconnecting cable. The cable pin-out is:

HP 25-PIN CONNECTOR	Series 35 PLUS J107 (or J108)	SIGNAL
1	21	PLTY
2	4	YGND
6	14	Ground
14	23	PLTX
15	2	XGND
HP 9-PIN CONNECTOR		
2	5	SEEK
3	14	Ground
4	6	CPC
5	9	NABL

5.7.4 Model C1513 General Purpose X-Y Plotter Cable

25-Pin Connector	Wire Color	Plug Color	Signal
21	Red	Red	PLTY
4	Orange	Black	YGND
23	Blue	Red	PLTX
2	Green	Black	XGND
14	Black	Black	Ground

5.8 MODEL 3553 Graphics Plotter

The Model 3553 Graphics Plotter Interface can be used with the Hewlett-Packard HP 7470A (Canberra Model 5207A) two-color Graphics Plotter. It can also be used with the HP 7225, with 7603 Personality Module and the HP 7220 Plotters (former Canberra Models 5207 and 5206).

The Plotter Interface is set to the Line Plot mode. To change the mode to Point Plot, refer to the instructions for the interface's M-N jumper in appendix A.8.

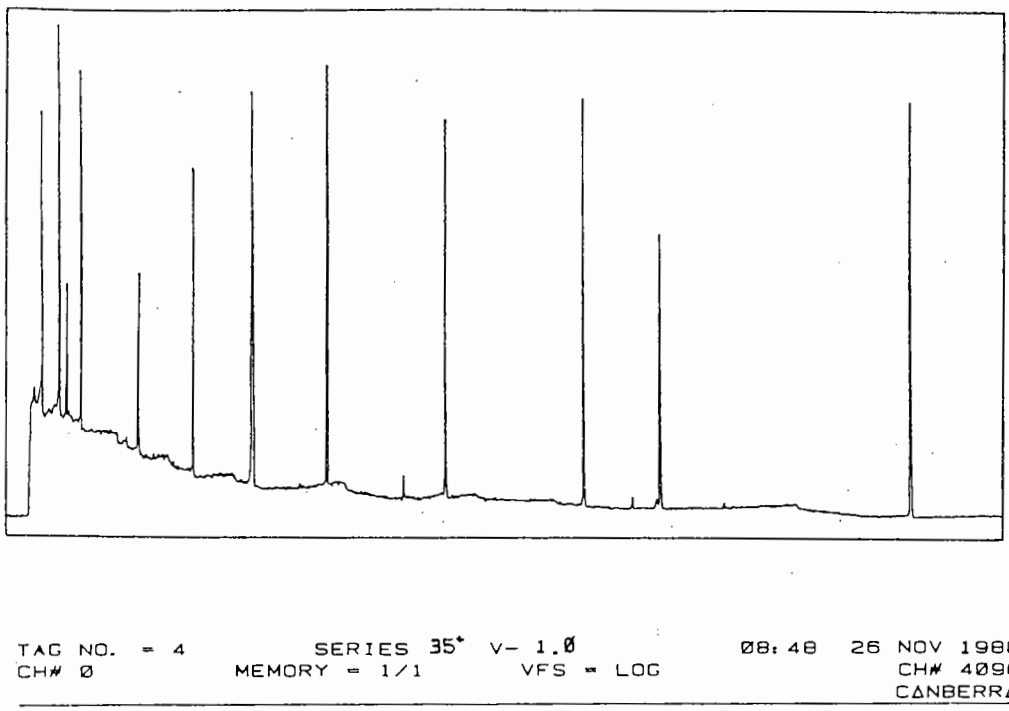


Figure 5.4
Typical X-Y Plotter
Readout

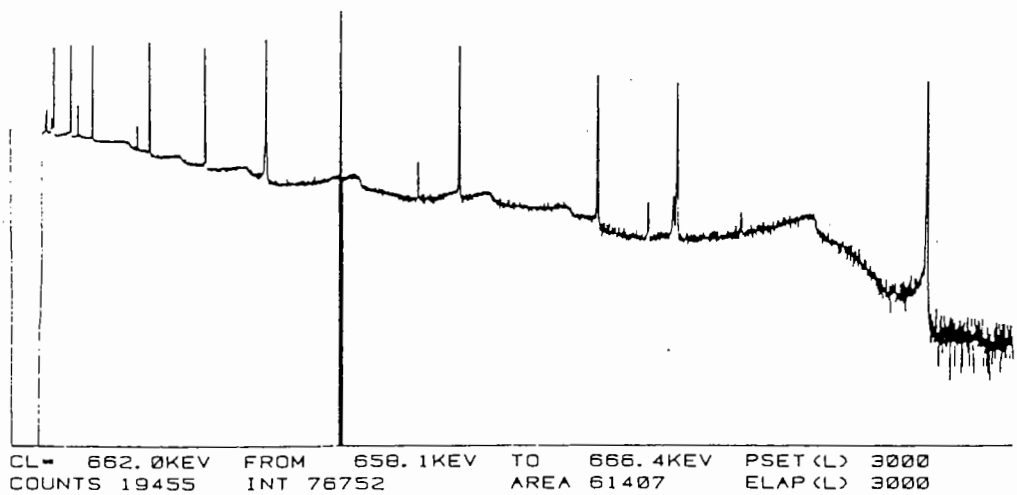


Figure 5.5
Typical Graphics
Plotter Readout

5.8.1 Model 5207A Setup

The Model 5207A Plotter's rear panel has an 8-pole rocker switch:

Pole	Setting
S2	0
S1	0
D/Y	1
A4/US	1
B4	1
B3	0
B2	0
B1	0

Refer to the HP operator's manual for the meaning of these switches and for specific instructions on plotter setup.

Connect one end of the supplied cable to J107 (or J108) on the Analyzer and the other to the Plotter's EIA connector.

5.8.2 Plotter Operation

When the Plotter is set up and connected to the Analyzer, press READ OUT and select GRA as the readout device. Now press YES to start the readout.

The Series 35 PLUS must be on before the Plotter is turned on to assure proper operation.

The Plotter will read out the alphanumerics and the spectrum currently displayed. The MEMORY switch and AREA/INTEGRAL, ECAL, and USE, if desired, must be selected before starting the readout.

Figure 5.5 shows a typical Graphics Plotter readout.

5.9 OTHER I/O DEVICES

Operation of options 3552A, 3554, 3571, 3572 and 3573 is explained in the separate manuals for each of these devices.

SECTION 6
TASK (LEARN/EXECUTE)

The Series 35 PLUS Task function offers a means of defining and automatically executing a Task. That is, a sequence of Analyzer functions.

- Up to four tasks can be entered.
- Any one task can be executed at a time.
- While the task is in progress, no analysis or control functions are available to the operator. Display functions can still be enabled, however.
- Any running task can be stopped manually.
- A task may be entered manually (LEARN) or by way of a previously learned task which has been stored externally (LOAD).
- A Define/Use equation may be entered as a step by pressing ANALYZ during task entry.
- The data collection mode (PHA or MCS) can't be learned. The mode must be manually set before Execute is enabled.

Table 6.1
Bytes per Function

Analyzer Function	Dialogue Mnemonic	Bytes Used
CLEAR DATA	CLRDATA	2
CLEAR ROI	CLRROI	2
CLEAR TIME	CLRTIME	2
COLLECT	COLLECT	2
ENTER ROI[1]	ENTROI	6
PEAK[2]	PEAK	2
PRESET MCS	PSET MCS	5
PRESET PHA	PSET PHA	11
READ IN	READIN	4
READ OUT	READOUT	5
SMOOTH	SMOOTH	3
STRIP	STRIP	5
TRANSFER	TRANSFER	3
USE EQUATION #n[3]	USE EQU #n	2

The notes refer to sections E.1, E.2, and E.3 on the next page.

6.1 TASK RULES

A task is Learned (entered manually) by pressing the key associated with the desired function and completing the dialogue associated with that function. During the Learning process, the following rules apply:

A. Entering a task manually (LEARN) is simply a process of responding to the dialogue presented by the analyzer for each function.

B. Each task may occupy up to 64 bytes of memory. See table 6.1.

C. The number of bytes remaining for the task will be displayed at the right side of the dialogue portion of the display (TO GO =).

D. After entering a step, a response of YES will move the task on to the next step.

E. The learning process will terminate if the operator presses TASK again, disabling the function and erasing all entered steps.

E.1. In the ENTER ROI dialogue, press STORE to enter the current cursor location (channel) or enter a channel number.
E.2. Choose Peak Sigma before executing a task. For correct peak search in a task, all ROIs in the memory must be cleared first. They may be cleared manually or by a task step.
E.3. An equation must be defined before entering it as a task step.

F. If the dialogue asks if the current memory segment, as selected by the MEMORY switch, is acceptable; the only response that can be made is YES. To change to another segment, the function must be turned off, the MEMORY switch changed to another position and the function turned on again.

G. When task entry is complete, the dialogue allows the operator to save the task on a peripheral recording device (section 6.5).

H. Storing a task externally is accomplished by reading out a binary-encoded record to a Cassette tape, to a punched paper tape (TTY), or to any EIA device that can record binary data.

I. If LOAD (from an external device) is selected instead of LEARN, the operator may select TTY (Teletype) or CASsette as the device to Load from. A response of YES starts the Loading readin.

J. If, in entering a task, all of the available bytes of memory are used, an attempt to enter another step will cause the message NO ROOM to be displayed. Pressing CLR will remove the message from the display and allow the operator to exit the task dialogue.

The steps are displayed only as each one is learned, so it might be helpful to make a list of the steps before entering them into a task. This will ensure that the correct steps are entered in the proper order.

At the beginning of the task, and again as each step is entered, the display shows "GO TO 1". This command, which uses 2 of the 64 bytes, is included in every task as the final step. This allows the task to be repeated from a given point (in the default case, from step one) in multiple runs of the task.

6.2 ENTERING A TASK

Pressing TASK will show:

```
*ENTER   EXECUTE
           OK?
```

Any entered task may be executed; refer to section 6.7.

To enter a task, answer YES to ENTER. The dialogue will change to:

```
*TASK#1
X=              OK?
```

The task number can be changed to 2, 3, or 4 at this point.

Pressing YES in answer to OK? will show:

```
*LEARN   LOAD
              OK?
```

The operator must choose to enter a task manually (LEARN) or by way of a previously recorded task (LOAD).

6.3 LOADING A TASK

A YES answer to LOAD will allow the choice of I/O device to read the task in from:

```
DEV= TTY  *EIA
              OK?
```

Pressing YES again will start the Readin.

6.4 LEARNING A TASK

A YES answer to LEARN yields:

```
STEP #1    GO TO 1
X=            OK?            TO GO = 62
```

At this point the operator may change the GO TO command from Step 1 to any other step, as desired.

Note that "GO TO" uses 2 of the 64 bytes.

To enter a function as step number one, press the key associated with the desired function. For instance, CLEAR DATA, which will start the task with a cleared memory.

The display will ask if the currently selected memory segment is acceptable for the operation:

```
FULL
                OK?
```

Note: See general rule "F" at the beginning of this section.

Press YES to accept this step. The display will revert to:

```
STEP #2   GO TO 1
X=
                OK?          TO GO = 60
```

Step number two may now be entered and the GO TO command may be altered, if desired. This dialogue will be displayed at the completion of every step, changing only the step number for the next succeeding step and the bytes TO GO total.

After entering all desired functions into the task, up to the limit of 64 bytes of memory per task, the operator will answer YES (to OK?) to exit the task dialogue.

6.5 SAVING A TASK

After the task has been defined, it may be recorded externally to be read and used at another time.

Answering YES will change the dialogue to:

```
SAVE TASK # 1
             OK?
```

Pressing NO bypasses the SAVE operation, leaves the task in memory, and returns the display to normal. A response of YES gives the operator the choice of recording device:

```
DEV  TTY  *EIA
                OK?
```

Pressing YES allows the binary-encoded readout to start.

6.6 EDITING A TASK

After the task has been entered and accepted, it can be corrected by deleting incorrect steps or by adding omitted steps. To start the Editing process, press TASK and YES to see:

```
*TASK # 1
X=            OK?
```

The operator can change the task number through the X Register or can accept the displayed number. Pressing YES will show:

```
*LEARN  LOAD
                OK?
```

Accepting the Learn mode will show a new dialogue line:

```
USE OLD
                    OK?
```

Answering NO will delete the entire task; answering YES will allow the operator to review the task step by step, correcting as necessary:

1. Using the plus key (+) will advance through the sequence one step at a time.
2. Using the minus key (-) will back up through the sequence one step at a time.
3. Using the NO key will delete the currently displayed step.
4. Another step may be entered in the usual manner.
5. Instead of entering a new step, + or - may be pressed to go on with the editing process.
6. During the editing process, the task will show the total number of bytes left in the task (TO GO=). This number will change only if a step in the task is changed to one using a different number of bytes or if a step is added or removed.
7. If enough bytes remain, new steps may be entered at any point in the current sequence. New steps will be inserted before the displayed step.
8. When editing is complete, answering YES to the OK? will display the SAVE TASK dialogue as in section 6.5.

6.7 EXECUTING A TASK

To begin the sequence, the operator presses TASK, selects EXECUTE, and responds to two questions:

```
*TASK # 1
X=              OK?
```

The task number can be accepted or changed through the X Register. YES brings up:

```
*CYCLES=1
X=              OK?
```

The X Register here allows the operator to change the number of cycles of task repetition from one to any desired number between two and 255. If indefinite repetition is desired, enter 0. The task will recycle until aborted. (See section 6.8.)

A response of YES starts the execution of the task.

Note that the Execute function cannot be enabled while the analyzer is in Collect, Readin or Readout.

6.8 STOPPING A TASK

To stop an active Task, press TASK. The dialogue will show:

```
*ABORT  STOP          CYCLES=nn
                           OK?
```

Abort

ABORT will stop the Task immediately. If MCS collect is the current step, the task will continue to the end of the current sweep.

Stop

STOP will stop the task at the end of the current cycle.

Note that the number of cycles remaining to be run is also displayed. If you want only to check the number of cycles remaining, press TASK once more. This response will allow the Task to continue. Be careful not to press YES at this point or the Task will be aborted.

SECTION 7
MODELS 3541x STANDARD AND OPTIONAL DEFINE/USE/AP-PAKS

The optional DEFINE/USE allows the operator to enter and use, either manually or from an external device, up to four algebraic equations. The equations may use one or two Constants and one or two Variables plus Live time (TL). All operations are performed in Floating Point arithmetic.

The AP-PAK part of the option provide 10 predefined equations for solving common analysis problems. The AP-PAKs are covered in detail in section 7.12.

The equations are accessed by pressing the front panel ANLYZ key. Analyze comprises six functions, each covered in a separate section:

Editing (7.2) Define (7.3) Save (7.4) Use (7.5) Load (7.6) Acc (7.7)

7.1 EQUATION RULES

1. Parenthetical nesting is provided up to four levels.
2. An equation may be a maximum of 57 displayed characters. Note that some operations require more than one character: Square Root, for instance, is displayed as SQRT: a total of 4 characters of the 57 available.
3. Computation is performed according to the hierarchy of operations shown in the following list. Within a given level, computation is performed from left to right.

Operation	Hierarchy
√ (SQRT) ex (EEX) Unary minus (-)	First level
Multiplication (*) Division (/)	Second level
Add (+) Subtract (-)	Third level

4. In addition to the usual operators, the Series 35 PLUS provides exponential notation to the base e (natural logarithm), as well as to the base 10. The EEX key on the keypad is used for both bases.

   The Firmware picks which base to use by the following rules:

   A. If a numeric entry precedes the EEX, the Firmware will use the base 10. That is, an entry of 4.7, EEX, 4 will be read as 4.7×10^4. It will be displayed as 4.7E4.

   B. If there is no number preceding the EEX, the Firmware will use the base e. That is, an entry of 5, X, EEX, 3 will be read as 5 times e^3. It will be displayed as 5 X EXP3.

      Note that the exponential notation on the display varies with each base: when the base ten is raised to a power, the display shows "E"; when the base e is raised to a power, the display shows "EXP".

5. Constants may be defined for each equation as K1 or K2 or entered as numeric literals in integer, fixed decimal, or exponential format. Constants are always displayed exponentially; base e cannot be used.

6. Each equation may have two variables, which are defined as:

   1. CL#: The current Cursor Location (channel number). If the spectrum is energy calibrated, energy units rather than a channel number will be used in the calculation.

   2. CNT@CH#: The count in a specified channel. A specific channel number may be entered, or STORE may be pressed to enter the channel number of the current cursor location. Entering channel zero as the channel number will be interpreted as the current cursor channel.

3. INTG#: Integral of a specified ROI. Entering zero as the region number will be interpreted as the current ROI. If more than one ROI has been entered, the ROIs are counted from left to right to signify which ROI# is being referred to.

   Current ROI is defined as the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

4. AREA#: Area of a specified ROI. ROI defined as in Step 3.

5. EQ#: The current value of the specified equation. This function allows equations to be chained: If the current equation needs to have more than two Variables, further Variables can be defined in another equation and referred to with this function. Reference to the current equation number is not legal.

6. CENT#: The peak centroid of a specified ROI. ROI defined as in Step 3.

7. FWHM#: The full width half maximum of a specified ROI. ROI defined as in Step 3.

7.2 EDITING

As the equation is entered, a mistaken entry can be deleted by pressing NO, which will delete the most recent entry. If the mistake is several entries back in the equation, it may be deleted by pressing NO several times, which will erase each final entry. When the mistake has been deleted, the correct entry can be made and the equation continued.

In addition, the entire equation may be erased by pressing the CLR key.

7.3 DEFINE

Pressing the ANLYZ button reveals:

```
EQU#1
X=                OK?
```

The default equation number (1) may be changed to 2, 3, or 4 by way of the X Register. Pressing YES will show the next line of dialogue:

```
*DEFINE    USE    LOAD
                   OK?
```

Accepting DEFINE with a YES shows:

```
EQU#1
X=                OK?
```

The X Register is used to enter the desired equation. When the equation is complete, press STORE to transfer the equation to memory.

When the equation has been entered in memory (with STORE), press YES to bring up the next line of dialogue:

```
*K1  0.00E00      K2   0.00E00
X=                OK?
```

If either K1 or K2 was specified as part of the equation, they will be defined here, using STORE. Press NO to advance the * to K2 and enter if required.

If neither was specified as part of the equation, this section may be disregarded. In either case, pressing YES will reveal:

```
V1= CL#  CNT@CH#  INTEG#  AREA#  EQ#  CENT#  FWHM#
X=                  OK?
```

If Variable one (V1) was specified in the equation, it will be entered here. If not specified, press YES to go on to the dialogue for variable two (V2), which uses the same format.

When the two Variables have been entered, pressing YES will reveal:

```
    SAVE EQU #n     OK?
```

The displayed equation number is the number of the current equation. NO will terminate the dialogue. YES will allow the choice of devices for saving the equation.

7.3.1 Redefine

If ANLYZ is pressed again after entering an equation, the same initial dialogue is displayed; after DEFINE is accepted with a YES, a new line of dialogue will be displayed:

```
    USE OLD EQU # n
                    OK?
```

The current equation "n" will be displayed in the X Register. If it is to be retained, pressing YES will allow the dialogue for the equation to proceed. If NO is pressed, the current equation will be deleted from memory, allowing a new equation to be entered in its place. If ANLYZ is disabled at this point, the equation will no longer be available.

If YES is pressed, to USE OLD equation, the dialogue will go on to the Constant parameters that were entered for the equation so that they may be altered if desired.

Pressing YES to accept the existing, or the altered, Constant parameters will allow the dialogue to proceed to the first of the Variable parameters for review as with the Constant parameters.

Pressing YES again will bring up the second of the Variable parameters for review and pressing YES once more will show the SAVE dialogue. (See Section &.3)

7.4 SAVE

Once an equation has been entered in memory, it can be saved by reading it out to an extermal device. Answering the SAVE dialogue (at the end of the Define dialogue) with a YES will reveal:

```
DEV=   TTY   *CAS
```

After selecting the appropriate readout device, press YES to start the readout. Pressing NO bypasses the SAVE operation, leaves the equation in memory and returns the display to normal.

7.5 LOAD

To enter an externally recorded equation into memory, the Load feature is used. The second line of the Define dialogue allows the choice of Learn, Load or Use. Answering YES to LOAD shows:

```
DEV=   TTY   *EIA
```

After selecting the appropriate readin device, press YES to start the readin.

7.6 USE

To Use an entered equation, press ANLYZ, enter the desired equation number using STORE, then YES. This brings up:

```
*DEFINE    USE    LOAD
```

Select USE, then press YES to enable the selected equation. The result of the equation will appear in the lower right part of the display, in place of Preset, as USER=.

As data is accumulated, the equation will repeatedly be evaluated and the display updated.

Note that the program converts the decimal entries to a digital form for manipulation and then convert back to decimal form for display. The conversion process has a small rounding off error, but the displayed evaluation results are accurate to at least ±1 least significant digit.

7.7 ACCUMULATOR

Define/Use also includes a floating point register that can be used as an accumulator (ACC) of instantaneous equation results. When USE is enabled, the Accumulator can be enabled by pressing STORE, which will allow the register to be used to keep a running total of the results of the equation's continual evaluation of the data.

Mathematically, the Accumulator will perform ACC = ACC + VAL each time STORE is pressed, where VAL is the equation value currently displayed in the USER register. This feature can be used to sum the results of several equations or of several runs of one equation.

7.8 RESULTS IN A READ OUT

If USE is enabled when a Read Out is started, the current equation will be printed in the Report Header, along with the values for the Constants and Variables for that equation. If ROI # n is specified, the results of the equation for that ROI will be printed in the Header. Figure 7.1 shows a typical Define/Use readout.

If the equation contains a reference to ROI # 0 (the current ROI) and the Read Out is a ROI type, the equation will be re-evaluated for each ROI and the equation's value will be included in the data summary for each ROI.

Current ROI is defined as the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

Note that if either of the Variables is not defined, it will be shown in the readout as V1 (or V2)=CL, the default state for the Variables.

```
TAG NO  =        4       3541 ROI BRIEF READOUT                    PAGE    1
MEMORY= 1/2  LIVE TIME=      4000 TRUE TIME=      4080     3 APR 84  13:31

EQU# 1 =(V1-V2)/V1
K1= 0 00E00       K2= 0 00E00       V1=INTG#0     V2=AREA#0
USER= 0 73025E00

ROI#   1  FROM      162 CH#  TO      179 CH#        USER   0 73025E00
          INTEGRAL      31218        AREA      8471
          CENTROID   0 16909E03      FWHM   0 30677E01

ROI#   2  FROM      236 CH#  TO      252 CH#        USER   0 55247E00
          INTEGRAL      40248        AREA     18012
          CENTROID   0 24354E03      FWHM   0 31076E01

ROI#   3  FROM      333 CH#  TO      347 CH#        USER   0 63671E00
          INTEGRAL      23876        AREA      8674
          CENTROID   0 33968E03      FWHM   0 32649E01

ROI#   4  FROM      583 CH#  TO      596 CH#        USER   0 49771E00
          INTEGRAL      17443        AREA      8760
          CENTROID   0 58606E03      FWHM   0 31656E01

ROI#   5  FROM      826 CH#  TO      844 CH#
          INTEGRAL      18504
          CENTROID   0 83446E03
```

Figure 7.1
Define/Use
Brief Readout

7.9 SAMPLE EQUATION

One useful equation that might be entered is the one that defines the percent error (%ERR) of the integral of a given region. This equation will be used to show how a complex equation can be entered with the Define/Use option. The equation reads:

$$\%ERR=1.65x100(INT+((N\div2)^2(A+B)))^{1/2}\div(INT-((N\div2)X(A+B)))$$

Where
- N = the number of channels in the region being evaluated,
- A = the number of counts in the last channel before the region,
- B = the number of counts in the first channel after the region,
- INT = the integral value of the region.

To enter this equation in a form acceptable to the firmware, it must first be slightly altered and entered as:

$$K1\ X\ \sqrt{(V1+(K2\ X\ K2\ X\ V2))}\ \div\ (V1-(K2\ X\ V2))$$

Where K1 = 1.65, for a 90% confidence level, X 100
- V1 = Integral of the region,
- K2 = (N ÷ 2),
- V2 = (A + B).

Since A and B are also variables and since the equation only allows for two variables, which have already been defined, they must be entered in a second equation. The second equation, EQU#2, can be defined as V1 + V2, which will correspond to A and B of the first equation.

In entering K2, the evaluative feature of the X Register, mentioned in section 2.3.4, can be used. Enter the ROI's Stop channel number minus Start channel number plus one, divide by 2 and STORE. For example, 419-342+1÷2 will be evaluated and stored as 39.

7.10 USER PRESET

To use a defined equation as a Preset condition, press PRESET to see:

```
*TIME (L) TIME (T) COUNTS INT AREA USER VAL = n
X=                    OK?
```

The value "n" displayed will be the last entered Preset. Advance the * to USER with the NO button and press YES to see:

```
   *USER = n    EQU#1
    X=              OK?
```

The desired value for the Preset can be entered through the X Register while the * is at USER. Press NO to advance the * to EQU# to enter the appropriate Equation number for the Preset function to evaluate, then press YES to terminate the dialogue. The Preset portion of the normal display will now show "PSET (U) =".

Since the Preset is an increasing function, using the % Error equation of section 7.9 will require a change in the equation (% Error is a decreasing function). Simply change the equation to "10-(equation)" and enter the Preset value as the difference between 10 and the desired value. For instance, if data acquisition is to stop when the % Error has decreased to 7%, enter the Preset value as 3, the difference between 10 and 7 (the desired value).

Enabling COLLECT will allow the acquisition to continue until "ELAP (U)" equals 3. Note that the Elapsed value will start as a negative number, because the initial % Error value will be greater than 10. When the Elapsed value has increased to 3, acquisition will stop.

If a Preset is to be used that is not expressed as a percent but is a decreasing function, the Equation must be defined as "(10-equation) ÷ 100."

7.11 OPERATOR'S EQUATIONS

Use this space to make notes for your own equations.

7.12 THE OPTIONAL AP-PAKS

The standard Model 3541 Ap-Pak is described in section 7.13. Appendix F contains a full listing of the 3541's equations.

The Model 3541C Chromatography Ap-Pak and the Model 3541N Nuclear Medicine Ap-Pak are covered in separate manuals.

These optional Ap-Paks extend the capability of the Define/Use option by providing the predefined functions, each of which will solve a common analysis problem. These equations, numbered 5 through 14, are a part of MCA program memory and will not be lost when power is turned off.

Any defined equation can be accessed by pressing ANLYZ to see:

```
*EQU #1
X=              OK?
```

Enter the Ap-Pak equation number through the X Register. This displays:

```
*DEFINE   USE   LOAD
                OK?
```

Select DEFINE to view the selected equation. If the equation contains constants K1 or K2, these must be defined using the X Register.

To Use an Ap-Pak equation, follow the procedure of section 7.6, using the X Register to enter the desired equation number.

7.13 THE STANDARD AP-PAK (3541)

Table 7.1
Standard Ap-Pak Equations

Number	Name	Callout
5	Minimum Detectable Activity	MDA
6	Compton Edge	COMPT
7	Counts per second	CPS
8	Percent Error of an Area	%ERR
9	Percent Dead Time	%DT
10	part of equations 11 and 13	HLIFE see note
11	Efficiency	EFFIC
12	Activity in µCuries	ACTIV see note
13	Decay Corrected Activity	DCACT see note
14	Dose Rate in mR/hr	DOSE see note

NOTE:

Equation 10 is used to enter the half life for equations 11 and 13. Equation 12 uses the results of equations 10 and 11. Equations 13 and 14 use the results of equations 10, 11, and 12.

Equations 6 through 9 are complete; no further entry is required. Equation 5 and equations 10 through 14 need more data: The values for K1 and K2 must be entered manually before the equation can be solved.

Current ROI means the ROI in which the cursor is located. If the cursor is Indexed to another ROI, the equation will be recalculated for that ROI.

#5 Minimum Detectable Activity

Calculates the lowest detectable activity in microcuries for the current ROI. Enter:
K1 = Gammas per disintegration for the isotope being analyzed.
K2 = The results of Equation #11.

#6 Compton Edge

Calculates the Compton Edge for the current ROI in a keV energy calibrated spectrum.

#7 Counts per Second	Calculates CPS for all of the displayed spectrum or for the current ROI if one has been entered.
#8 Percent error	Calculates the % error of the Area of the displayed spectrum or of the current ROI if one has been entered.
#9 Percent dead time	Calculates the spectrum's dead time to several decimal places.
#10 Half life for #11 and #13	K1 = Half life of the isotope being measured.
#11 Efficiency	Calculates the detector's efficiency at the energy of the current ROI. Enter: K1 = Gammas/sec for energy being measured. K2 = Decay time in the same time units as the half life in equation 10.
#12 Activity	Calculates the current ROI's activity in microcuries. Equations #10 and #11 must be completed first. Enter: K1 = Gammas per disintegration. K2 = The results of equation 11
#13 Decay Corrected Activity	Corrects equation 12 for decay. Equations #10, #11, and #12 must be completed first. Enter: K1 = Decay time of the isotope in the same time units as the half life in equation 10.
#14 Dose Rate	Calculates the dose rate in milliroentgens per hour for the current ROI. The spectrum must be Energy Calibrated in keV. Equations #10, #11, and #12 must be completed first. Enter: K1 = Yield (gamma quanta per disintegration). K2 = Detector to source distance in meters.

SECTION 8
MODEL 3543 ISOTOPE ANALYSIS
MODEL 3544 X-RAY ANALYSIS

Model 3543 allows the user to perform qualitative isotope analysis on a spectrum. Using the included Isotope Library, the user can identify unknown isotopes in a spectrum. Model 3544 allows analysis of an X-ray spectrum for K, L, and M lines.

Appendix G lists the Isotope Library and Appendix H lists the X-ray Library.

Using the Option

To use the ISO ANLYZ function, the MCA must first be Energy Calibrated. ISO ANLYZ allows the user to select the window width, in energy units, that will be used to evaluate the spectrum. The user also has the option of selecting MANUAL or AUTO operation.

Manual Mode

In MANUAL mode, moving the SCAN control steps the Series 35 PLUS through its Isotope Library, displaying the chemical symbol and atomic mass number of each library entry in turn at the bottom of the screen.

Blinking cursors are positioned at each expected peak location. If every blinking cursor has a peak associated with it, this isotope is present in the spectrum. If all cursors do not coincide with a peak, turn the SCAN control so that the next isotope name and its cursors appear on the display. This process should continue until a match is found or the library has been exhausted (indicated by END appearing in place of an isotope name).

Auto Mode

In AUTO mode, moving the cursor to a spectrum peak will cause the program to attempt to match the energy at the cursor location, plus or minus a previously selected energy window, to the energy of the isotope in the library. If a match is found, the name and energy of the isotope will be displayed and blinking cursors will be placed at all locations where a peak is expected.

The user should then examine the blinking cursor locations to see if there is a peak under each one. If each cursor matches a peak, then this isotope is present in the spectrum.

Readouts

Figures 8.1 and 8.2 illustrate the results of a hard copy readout for each of the options.

8.1 3543 MANUAL MODE

To use ISO ANLYZ, the spectrum must be ECAL'ed (section 4.13). Once this is done, ISO ANLYZ can be selected. The first time the ISO ANLYZ key is pressed, the display will ask:

```
WINDOW (KEV  ) = 0.0
X =     OK?
```

The desired search-window width can now be entered using the X Register dialog. KEV must be entered as whole numbers. If the MCA is calibrated in EV, the display will show WINDOW (EV) = 0.0 and the value entered in the X Register will be interpreted as 100's of EV.

Once the search-window has been selected, ISO ANLYZ will be disabled. Pressing ISO ANLYZ again will now cause the display to show:

```
SCAN-MODE *AUTO    MANUAL
```

Pressing NO, then YES, will select MANUAL operation. Note that once the search-window has been selected, its value will remain unchanged and the ISO ANLYZ dialog will go directly to SCAN-MODE until a new ECAL is performed or a system reset occurs.

The display will now show:

```
NA-22
```

Blinking cursors will appear at the two locations where Na-22 peaks should be if the isotope is present. If these blinking cursors coincide with peaks, Na-22 is present. If both blinking cursors do not fall on peaks, Na-22 is not present.

Turning the SCAN control clockwise will cause the next library isotope and its cursor(s) to appear on the display. The user can continue to SCAN the library in this manner for other isotopes until END appears on the display. The library can be SCANned in either direction by turning the SCAN control clockwise or counterclockwise.

8.2 3543 AUTO MODE

AUTO operation is begun in the same manner as MANUAL except that the user now responds with YES to the AUTO mode.

If the PEAK function is not enabled, move the cursor to a spectrum peak and press ISO ANLYZ again. This causes the MCA to search its library for any isotope with a peak whose energy falls within plus or minus the search-window from the current cursor position. If such an isotope is found in the library, its name and energy are displayed on the screen as follows:

CO 60 AT 1173.2

Blinking cursors will now appear at each location where an isotope peak is expected. If peaks occur at all of these locations, the isotope is present in the spectrum.

Pressing ISO ANLYZ again will cause the MCA to continue to search the library until either another isotope at this energy is found or the END of the library is reached.

If the cursor is moved while the function is enabled, pressing ISO ANLYZ again will restart the library search from the beginning. The new cursor energy will be used as the search target.

When END is seen on the display, the user may press ISO ANLYZ again to disable the function or move the cursor to a new location and press ISO ANLYZ to search the library for the new cursor energy.

If ROIs are present in the display, the user may enable PEAK before beginning ISO ANLYZ. PEAK has no effect on the MANUAL mode but can make the AUTO mode very easy to use. The ROIs may be the result of a previous PEAK search or may be user entered.

With PEAK enabled, ISO ANLYZ proceeds as before except that the library search is done at the centroid of the current ROI. This allows the user to INDEX the cursor to the next ROI and a new library search will automatically begin at the new centroid. If the user moves the cursor using the SCAN control, pressing INDEX will designate the current ROI as the one to the right of the cursor position. This allows the user to move the cursor past several ROIs without repeatedly pressing INDEX.

Note that the user may see two blinking cursors in one ROI if ISO ANLYZ is used with PEAK. This results from the possibility that the PEAK centroid and expected isotope location may be slightly different. These multiple cursors are more likely to be seen if the front panel WINDOW function is enabled.

8.3 3544 X-RAY ANALYSIS

The X-Ray analysis function works in a manner similar to the Model 3543 Isotope Analysis. The Front Panel dialog is the same as described in sections 8.1 and 8.2 with a few exceptions.

The first of these is that when the Model 3544 is installed, the ECAL dialog is changed to replace the MEV selection with KEV.3. This allows the user to specify energy in keV with 3 places after the decimal point. This maximum energy entry is limited to to 65.535 keV.

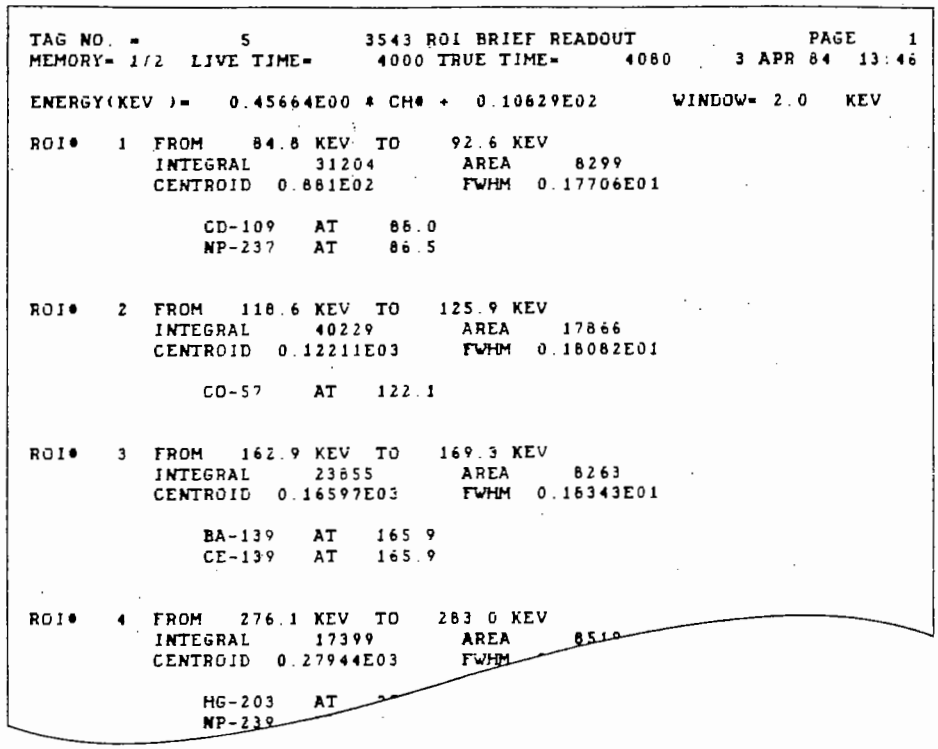
Manual mode operation is identical to the Model 3543 with the exception that the chemical symbol is followed by its atomic number rather than its mass number. Appendix H lists the Model 3544's X-Ray library.

Auto mode dialog is the same as described in section 8.2. If a match is found in the X-Ray library, the display will show:

```
ZR 40  KB1  AT  17.665  (18)
  |    |         |       |__intensity in %
  |    |         |_______energy in keV
  |    |_____________current K, L, or M line
  |__________element name and atomic number
```

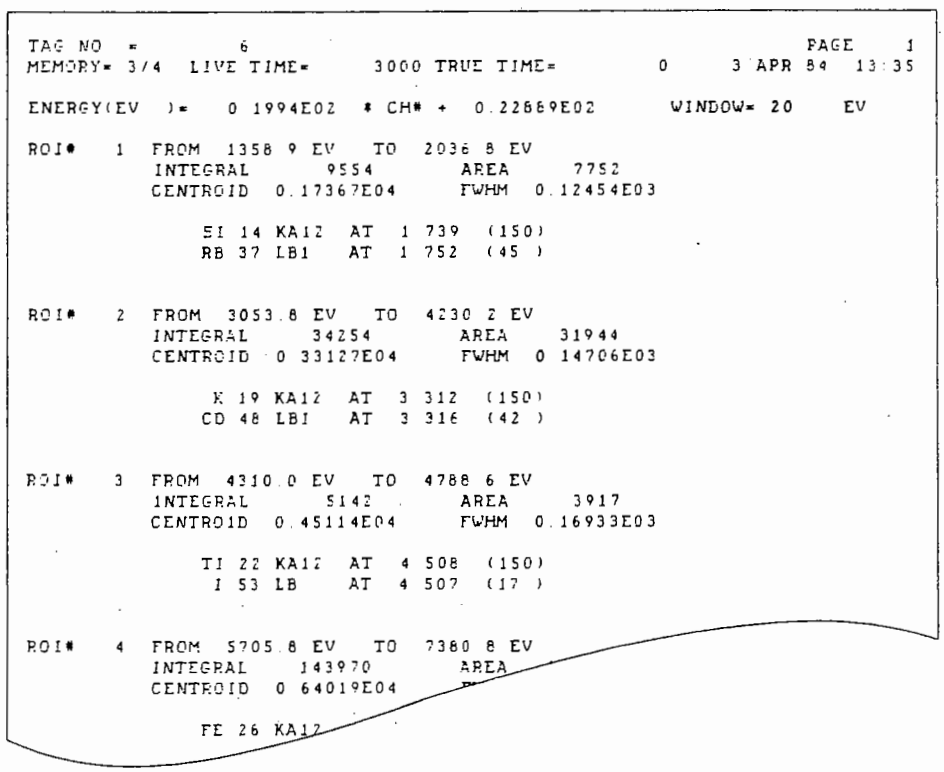
The reported X-ray intensities are relative to the current line.

Two signals are provided at the rear panel EXTERNAL CONTROL connector for the Model 3544. These are "Count in ROI" which provides a positive going pulse every time a count is stored in any ROI and "Count in Area ROI" which provides a positive going pulse when a count is stored in an ROI whose AREA is being displayed.



```
TAG NO. =        5          3543 ROI BRIEF READOUT                PAGE     1
MEMORY= 1/2  LIVE TIME=      4000 TRUE TIME=      4080     3 APR 84  13:46

ENERGY(KEV )=   0.45664E00 + CH# *  0.10629E02       WINDOW= 2.0    KEV

ROI#    1  FROM     84.8 KEV  TO     92.6 KEV
           INTEGRAL      31204        AREA      8299
           CENTROID  0.881E02         FWHM  0.17706E01

               CD-109    AT     88.0
               NP-237    AT     86.5


ROI#    2  FROM    118.6 KEV  TO    125.9 KEV
           INTEGRAL      40229        AREA     17866
           CENTROID  0.12211E03       FWHM  0.18082E01

               CO-57     AT    122.1


ROI#    3  FROM    162.9 KEV  TO    169.3 KEV
           INTEGRAL      23855        AREA      8263
           CENTROID  0.16597E03       FWHM  0.18343E01

               BA-139    AT    165.9
               CE-139    AT    165.9


ROI#    4  FROM    276.1 KEV  TO    283.0 KEV
           INTEGRAL      17399        AREA      8519
           CENTROID  0.27944E03       FWHM

               HG-203    AT
               NP-239
```

Figure 8.1
Isotope Analysis
Brief Readout



```
TAG NO  =        6                                          PAGE     1
MEMORY= 3/4  LIVE TIME=      3000 TRUE TIME=         0     3 APR 84  13:35

ENERGY(EV  )=   0 1994E02  * CH# +  0.22689E02       WINDOW= 20     EV

ROI#    1  FROM  1358 9 EV   TO  2036 8 EV
           INTEGRAL       9554        AREA      7752
           CENTROID  0.17367E04       FWHM  0.12454E03

               SI 14 KA12  AT  1 739  (150)
               RB 37 LB1   AT  1 752  (45 )


ROI#    2  FROM  3053.8 EV   TO  4230 2 EV
           INTEGRAL      34254        AREA     31944
           CENTROID  0 33127E04       FWHM  0 14706E03

                K 19 KA12  AT  3 312  (150)
               CD 48 LB1   AT  3 316  (42 )


ROI#    3  FROM  4310.0 EV   TO  4788 6 EV
           INTEGRAL       5142        AREA      3917
           CENTROID  0.45114E04       FWHM  0.16933E03

               TI 22 KA12  AT  4 508  (150)
                I 53 LB    AT  4 507  (17 )


ROI#    4  FROM  5705.8 EV   TO  7380 8 EV
           INTEGRAL     143970        AREA
           CENTROID  0 64019E04

               FE 26 KA12
```

Figure 8.2
X-ray Analysis
Brief Readout

SECTION 9
STANDARD AND OPTIONAL WIRING

The Series 35 PLUS includes as standard both External Control/Mössbauer wiring (section 9.1) and Pulse Pileup Rejection/Live Time Correction wiring (section 9.2).

The options are Model 3531A Mixer/Router wiring (section 9.3) and Model 3533 Digital Stabilizer wiring (section 9.4).

9.1 EXTERNAL CONTROL WIRING

External Control wiring provides for Remote Control of the Series 35 PLUS. TTL compatible signals on a rear panel 25-pin connector (J112) allow Mode and MCS Control, provide a Sample Changer interface, and provide signals for Mössbauer applications.

The signals on this connector are divided into five categories:

1. External MCS Signals--which function with the High Performance MCS.
2. Sample Changer Signals--which allow interfacing between the Series 35 PLUS and a Sample Changer mechanism.
3. Remote Control Signals--which allow external control of the Series 35 PLUS when the Serial Computer Interface (Model 3573) is not required.
4. Mössbauer--which allow interfacing to Mössbauer experiments.
5. X-ray analysis signals; option 3544.

Note that the signal receivers and drivers are not designed for rejecting >1 V of common mode or normal mode noise. If the interconnecting cable between the Series 35 PLUS and the remote control device is greater than 3 m (10 feet) in length, it may be necessary to use noise rejection to assure reliable operation.

Some noise rejection techniques that have been used successfully are:

RC filtering
Twisted Pair or Coaxial Cable
Terminating resistors
Level Shifting drivers and complementary receivers
Differential drivers and receivers
Opto-isolators

9.1.1 External MCS Signals

4 External Advance In--Logic 1 = High, Logic 0 = Low. With the MCS set for External Dwell time (section 4.27.2), the leading edge (↑) of the pulse advances the MCS address logic. In the Expand display mode, the minimum dwell is approximately 10 µs. In other modes, the minimum dwell time is 30 µs.

5 External Trigger In--Logic 1 = High or open, Logic 0 = Low. Minimum pulse width = 1 µs. Each MCS sweep will start when the External Trigger is at Logic 1.

22 AOF Out--Logic 1 = High, Logic 0 = Low. Pulse width = 12 µs to 18 µs. Generated at the end of each MCS sweep. The next sweep will start at the end of the pulse if the External Trigger is at Logic 1.

21 AMS IN--Logic 1 = High at 1 mA, Logic 0 = Low or open. Causes the MCS sweep to end and AOF to be generated. The sweep counter (channel zero) will be incremented.

15 Gate IN--Logic 1 = High at 1 mA, Logic 0 = Low. Can be used to enable the Gate function of the Series 35 PLUS. The function is determined by the ANTI/COINC jumper on the ADC board.

9.1.2 Sample Changer Interface Signals

8 Device Busy IN--Logic 1 = Low at 1 mA, Logic 0 = High or open. Collect can start only when this signal is at Logic 0, indicating that the Sample Changer is not busy. Collect will start about 30 ms after the signal goes to Logic 0.

6 Sample Changer Advance Out--Logic 1 = High, Logic 0 = Low. Pulse width = 75 ms to 125 ms. The Pulse is generated at the end of Collect, signalling that the Sample can be changed. The Device Busy In signal can be used to delay the start of the next Collect cycle.

9.1.3 External Control Signals

7 MCA Busy Out--Logic 1 = Low, Logic 0 = High. Indicates that the Series 35 PLUS is not able to accept an input command. Busy goes to Logic 1 during Readout and Clear Data.

9 Collect Status Out--Logic 1 = Low, Logic 0 = High. Indicates that the Series 35 PLUS is in the Collect mode.

10 Readout Status Out--Logic 1 = Low, Logic 0 = High. Indicates that the Series 35 PLUS is in the Readout mode.

11 Stop Collect In--Logic 1 = Low. Logic 0 = High or open. Maximum pulse width = 70 µs. If the pulse is received while the Series 35 PLUS is in Collect and not Busy, Collect will end on the next increment of Live time or at the end of the current MCS sweep. Functions with the Series 35 PLUS under Computer control.

12 Start Collect In--Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 µs. Input to start Collect within about 30 ms using current Preset and Function (PHA or MCS) in the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 35 PLUS is Busy or under Computer control.

13 Clear Data In--Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 µs. Input to clear data in the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 35 PLUS is Busy or under Computer control. Causes Series 35 PLUS Busy signal to go Low for about 200 ms.

25 Start Readout In--Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 µs. Input to start Readout with the current Readout parameters from the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 35 PLUS is Busy or under Computer control.

9.1.4 Mössbauer Signals

14 Address Advance Out--Logic 1 = Low, Logic 0 = High. Pulse width = 1 µsec nominal. Output pulse indicates MCS sweep has advanced to next channel.

16 Sweep Out--Logic 1 = High, Logic 0 = Low. Output level indicates that MCS sweep is active.

17	$SA2^{9}/$	Latched outputs from
18	$SA2^{10}/$	ADC Address Register
19	$SA2^{11}/$	Logic 1 = Low
20	$SA2^{12}/$	Logic 0 = High

9.1.5 X-ray Signals (Option 3544)

23 Count in ROI--Logic 1 = High, Logic 0 = Low. Pulse width 500 ns. Pulse occurs when count is stored in any ROI.

24 Count in Area ROI--Logic 1 = High, Logic 0 = Low. Pulse width 500 ns. Pulse occurs when a count is stored in ROI whose AREA is being displayed.

9.1.6 Signal Description

J111 (BNC)--COUNT INput for the Model 3522 High Performance MCS.

Logic 0 < + 0.3 V at 0 mA
Logic 1 > + 3.0 V at <1 mA
Pulse Width = 25 ns minimum
Pulse Pair Resolution = 50 ns minimum

J112 (25-pin Female D-style mating connector furnished)--EXTERNAL CONTROL connector. Signals on this connector are all TTL compatible.

All inputs
High = 2.4 to 5.0 V or open
Low 0.0 to +0.3 V at <2 mA
Pulse Widths >0.5 µs, except as noted.

All outputs
High + 2.4 to 5.0 V at <0.4 mA (2.4 V)
Low 0.0 to 0.5 V at <0.4 mA.

9.2 PUR/LTC WIRING

The pulse Pile Up Rejection and Live Time Correction (PUR/LTC) wiring adapts the Series 35 PLUS internal ADC for use with a Model 2020 PUR/LTC amplifier, or equivalent. The REJ jumper plug in the amplifier should be set for POSitive polarity.

The amplifier's PUR circuit inspects each input for the pulse pileup condition and permits the ADC to convert only single-event signals. If a pileup condition is detected, the REJ signal from the PUR circuit causes the ADC to discard this pulse. Refer to section A.11.11 for the signal description.

The ADC signals each acquisition (linear gate time) to the amplifier by signal LG. The rising edge of LG signifies that the pulse gate is now closed and the pile-up inspection circuit can be disabled. If a pulse has been rejected, the Live Time Correction circuit provides a busy signal (DT) to the Analyzer's live time circuit to correct for the additional dead time.

The amp's 3-pin PUR connector is connected to the S-35 PLUS's PUR connector (J116). The amp's DT connector is connected to the Series 35 PLUS's ADC BUSY connector (J117).

9.3 OPTIONAL MIXER/ ROUTER WIRING (Model 3531A)

This option allows the connection of a four-input Mixer/Router (Canberra Model 8222A or 8222B, or equivalent) to the Series 35 PLUS's Mixer/Router connector (J105). One Mixer/Router expands the single-input ADC to four inputs. Two or four Model 8222As may be connected to expand to eight or sixteen inputs.

The Mixer/Router, the Model 3521 ADC, and Model 3531A wiring combine to give multi-input PHA or MCS data acquisition capability to the Series 35 PLUS. Note: the Model 3522 High Performance MCS is single-input only.

The M/R key (section 4.22) on the Series 35 PLUS enables the MCA for routing. Pressing the key allows the operator to choose how many inputs are to be routed. With the M/R function enabled, the full memory will be equally divided between the selected number of inputs.

With two or four inputs, each input can be independantly started, stopped, or have its data manipulated.

With eight or sixteen inputs, the inputs are tied together in groups of four inputs each for starting or stopping data acquisition, or for data manipulation.

If only one input is to be used, the Mixer/Router should not be connected because its Dead Time and Inhibit signals can affect data storage.

The signal description for the Mixer/Router Wiring is listed in section A.11.3.

9.4 OPTIONAL DIGITAL STABILIZER WIRING (Model 3533)

The Model 3533 wiring option allows a Digital Stabilizer to be connected to the Series 35 PLUS's internal ADC through the J106 connector. The Stablizer can stabilize the ADC Gain, the ADC Zero, or both. The operation of the Analyzer with the Stabilizer is detailed in the Stabilizer's Operator's Manual.

The signal description for the Stabilizer Wiring is listed in section A.11.4.

SECTION 10
SIGNAL PROCESSING OPTIONS

The signal processing options available for the Series 35 PLUS are the Model 3521 AMP/ADC (section 10.1), the Model 3522 High Performance MCS (section 10.2), the Model 3523 Multi-ADC Interface (section 10.3), and the Model 3524 External ADC Interface (section 10.4).

10.1 MODEL 3521 AMPLIFIER/ADC

The Model 3521's use is covered in sections 2, 3, and 4 of this manual. It can be supplemented by the Model 3522 High-Performance MCS option or replaced by the Model 3524 External ADC Interface option or Model 3523 Multi-ADC Interface option.

10.2 MODEL 3522 HIGH-PERFORMANCE MCS

The Model 3522 High-Performance MCS option is used to allow a higher count rate in MCS operation. The standard MCS is limited to a count rate of about 20 kHz, maximum, while the Model 3522 allows an input count rate of up to 20 MHz. The Model 3522 is optional with the Model 3521 Amp/ADC, but must be used for MCS operation with the Model 3523 Multi-ADC Interface or Model 3524 External ADC Interface.

Refer to section 4.20 for MCS operation, to section 4.27.2 for MCS Preset, and to section 9.1.1 for external MCS control.

For this option, the output signal from an external high-speed SCA unit is connected to the rear panel's COUNT IN connector (J111).

Note that if the selected dwell time is equal to or less than 30 µsec, the data portion of the display will be blanked during High-Performance MCS Collect. This is done to allow the option more access time to the memory. The data collected will be visible on the screen when Collect ends.

10.3 MODEL 3523 MULTI-ADC INTERFACE

The Model 3523 Multi-ADC Interface allows up to four external ADCs to store PHA data in the Series 35 PLUS's memory. Each ADC is provided with Preset, start/stop Collect, Clear Data and Energy Calibrate functions. Independent Live and True Timers are provided for each ADC.

10.3.1 Setup

For ADC operating instructions, refer to the Operator's Manual for the ADCs being used. To connect the ADCs to the Series 35 PLUS, use the 25-pin cable supplied with each of Canberra's ADCs. A 25-pin cable can be made in the field by referring to the Signal List in section A.11.9.

On the Series 35 PLUS's rear panel, connect:

ADC # 1 to J106
ADC # 2 to J113
ADC # 3 to J114
ADC # 4 to J115

10.3.2 PHA Operation

The Model 3523 is capable of routing one, two or four external ADCs to the Series 35 PLUS's memory. To use more than one ADC, press the M/R button on the Series 35 PLUS's front panel to reveal the following dialogue:

```
NO. OF INPUTS   *2   4
          OK?
```

Select the number of inputs and press YES.

If a single external ADC is to be routed to the memory, do not enable M/R. This will allow ADC #1 to use the entire Series 35 PLUS's memory and store in the section determined by the position of the MEMORY switch when Collect is enabled.

If two inputs have been selected, ADC #1 will be stored in the first half of the memory and ADC #2 will be stored in the second half.

If four inputs have been selected, each ADC will be stored in one quarter of the memory, with ADC #1 in the first quarter, ADC #2 in the second quarter, and so forth.

The MEMORY switch allows control of the individual inputs. With the MEMORY switch in the 1/1 position, all ADCs will be started or stopped together.

If the MEMORY switch is in the 1/2 or 2/2 position, all ADCs assigned to that half of the memory will be started or stopped together. For instance, if two inputs are selected, either of the two ADCs may be started or stopped independently. If four inputs are selected, ADCs 1 and 2 or 3 and 4 may be started or stopped together. With the MEMORY switch in the 1/4, 2/4, 3/4, or 4/4 position, each of the four ADCs may be started or stopped independently.

In a similar manner, the MEMORY switch position will control the use of a region's Preset, Clear Data/Clear Time or Energy Calibrate functions.

Note that if the MEMORY switch is set to an inactive region of the memory, the display will show the Canberra logo. If the MEMORY switch is set to an active section of memory, the Dead Time Meter will be displayed, showing that the region is collecting.

The Series 35 PLUS's Firmware checks the ADCs at about a one microsecond scan rate to see if any ADC's conversion is complete. The first ADC found ready will have its converted address gated onto an address bus.

If the address is within the ADC's assigned range, is not inhibited by INHAD/ (see the Signal List in appendix A.11.9) and is not channel address zero or one, a PHA add one or subtract one cycle is performed. The Data Accepted signal is then generated to release the ADC for another conversion. Note that the address from the ADC must be stable during the entire memory cycle.

The ADC is prevented from storing an address beyond its assigned memory group. In order to minimize ADC dead time, the ADC's RANGE switch should be set to equal the assigned memory size for that ADC.

10.3.3 MCS Operation

Single-input MCS operates as described in the Multichannel Scaling operating instructions (section 4.20). To perform single-input MCS data acquisition, the M/R front panel function must be turned off and either the Model 3522 High Performance MCS option or an external MCS unit must be used.

A jumper plug on the Model 3523 Interface Board is provided for inverting the Count Enable Gate polarity. In the COINCidence position, an open connector (nothing connected) or a positive TTL level will enable counting; a TTL low level or ground will disable counting.

In the ANTIcoincidence position, an open connector or a positive TTL level will disable counting; a TTL low level or ground will enable counting.

10.3.4 Mixer/Router

The Model 8222 Mixer/Router can be used with any of the external ADCs to provide routing of up to 16 inputs to the memory. Using the Mixer/Router will allow its inputs to be routed to that ADC's memory segment. See the Model 8222 Operator's Manual for complete instructions.

Note: To use a Model 8220 Mixer/Router with the Series 35 PLUS, consult the factory.

10.3.5 Signals

Refer to figure 10.1 for PHA Cycle Timing Diagram.

Chassis connectors (J106, J113, J114, J115): female 25-pin; Amphenol type 17-10250.

Logic levels:
Logic Hi = +2.4 to +5 volts;
Logic LO = 0.0 to +0.3 volts.

10.4 MODEL 3524 EXTERNAL ADC INTERFACE

The Model 3524 ADC Interface allows an external Canberra ADC to store PHA data in the Series 35 PLUS's memory. The ADC is provided with Preset, Start/Stop Collect, Clear Data and Energy Calibrate functions. Live and True Timers are provided for the ADC.

10.4.1 Setup

For ADC operating instructions, refer to the Operator's Manual for the ADC being used. To connect the ADC to the Series 35 PLUS, use the 25-pin cable supplied with the ADC. A 25-pin cable can be made in the field by referring to the Signal List in section A.11.9.

On the Series 35 PLUS's rear panel, connect the external ADC to J106. Adjust the ADC's Gain, Range and Offset as desired.

10.4.2 PHA Operation

The ADC will store data in the MCA's memory as determined by the position of the MEMORY switch.

Gain, Range and Offset will be selected at the ADC.

The ADC is prevented from storing an address beyond its assigned memory group. In order to minimize ADC dead time, the ADC's RANGE switch should be set to equal the assigned memory size.

10.4.3 MCS Operation

Single-input MCS operates as described in the Multichannel Scaling operating instructions (section 4.20). To perform single-input MCS data acquisition, either the Model 3522 High Performance MCS option or an external MCS unit must be used.

A jumper plug on the Model Interface Board is provided for inverting the Count Enable Gate polarity. In the COINCidence position, an open connector (nothing connected) or a positive TTL level will enable counting; a TTL low level or ground will disable counting.

In the ANTIcoincidence position, an open connector or a positive TTL level will disable counting; a TTL low level or ground will enable counting.

10.4.4 Mixer/Router Operation

The Model 8222 Mixer/Router can be used with the external ADC to provide routing of up to 16 inputs to the memory. See the Mixer/Router Operator's Manual for complete instructions.

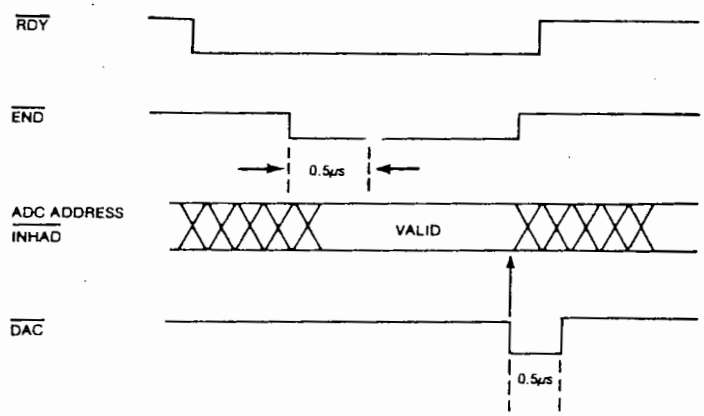


Figure 10.1
PHA Cycle
Timing Diagram

10.4.5 Signals

Chassis connector (J106): Female 25-pin; Amphenol type 17-10250.

Logic levels:
Logic HI = +2.4 to +5 volts;
Logic LO = 0.0 to +0.3 volts.

APPENDIX A
INTERNAL CONTROLS AND CONNECTORS

This appendix provides information that will be helpful in case of equipment malfunction. With common test equipment, such as an oscilloscope and a voltmeter, and reference to the information contained in this section, it will usually take no more than a telephone call or a letter to Canberra's Customer Service Department or your local Canberra Representative to quickly pinpoint the fault.

In the signal lists, negative true signals are shown with a slash (/) after the signal name. For instance, Dead Time is shown as DT/.

NOTE

Internal controls and jumpers that are not specifically mentioned in the following sections are either for test purposes or for factory installed options. They must not be moved.

A.1 OPERATING VOLTAGE SELECTION (figure A.1)

To change the operating voltage of the analyzer, move the plastic fuse shield, next to the ac line cord socket, to one side. The voltage selection printed circuit card (J4) is located just below the fuse. The operating voltage that the analyzer is set for will be visible on the card.

To change between 120 and 240 volts or to change to low-line voltage (100 or 220 volts), pull J4 out of its socket and replace it so that the desired voltage is visible beneath the fuse. A pair of needle-nose pliers is useful here.

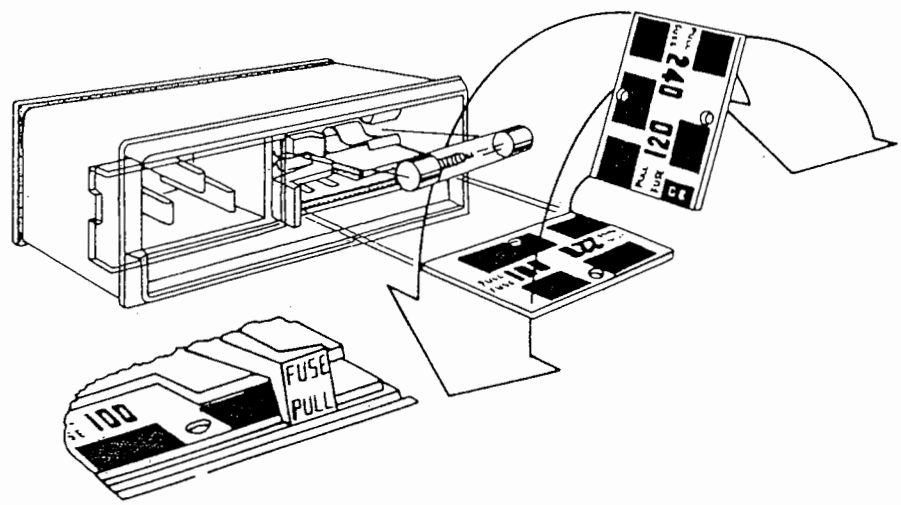


Figure A.1
Voltage Selection

Be certain to check the fuse rating when changing the operating voltage; a change from 100/120 volts to 220/240 volts, or the reverse, will require a change of fuse to the proper rating as well. See table A.1.

Table A.1
Series 35 PLUS Line Voltage Selection

Position	Operating Range	Line Fuse Rating
100	85 V to 110 V	1.5 A slow-blow
120	105 V to 130 V	1.5 A slow-blow
220	190 V to 240 V	3/4 A slow-blow
240	210 V to 260 V	3/4 A slow-blow

NOTE: For domestic operation at 220 volts, the supplied power cord should be replaced with an Underwriters' Laboratories listed, 220 V power cord, such as Belden's part number 17566.

A.2 CPU BOARD (figure A.2)

The D-E jumper supplies keep-alive power to the memory. Position D connects the on-board battery to the memory. Moving the jumper to E for about a minute, then back to D, will clear the memory and reset all parameters to factory default.

The 50 Hz wire jumper must be in place in areas using a 50 Hz line frequency and must be removed in areas with a 60 Hz line frequency. It defines the True Time clock's time base. If this jumper is changed, be sure to move the D-E jumper as mentioned in the paragraph above.

A.3 ADC BOARD (figure A.3)

AN/CO jumper selects ANticoincidence gating or COincidence gating. Shipped in the CO position.

PHA/SVA jumper selects Pulse Height Analysis or Sampled Votage Analysis. Shipped in the PHA position.

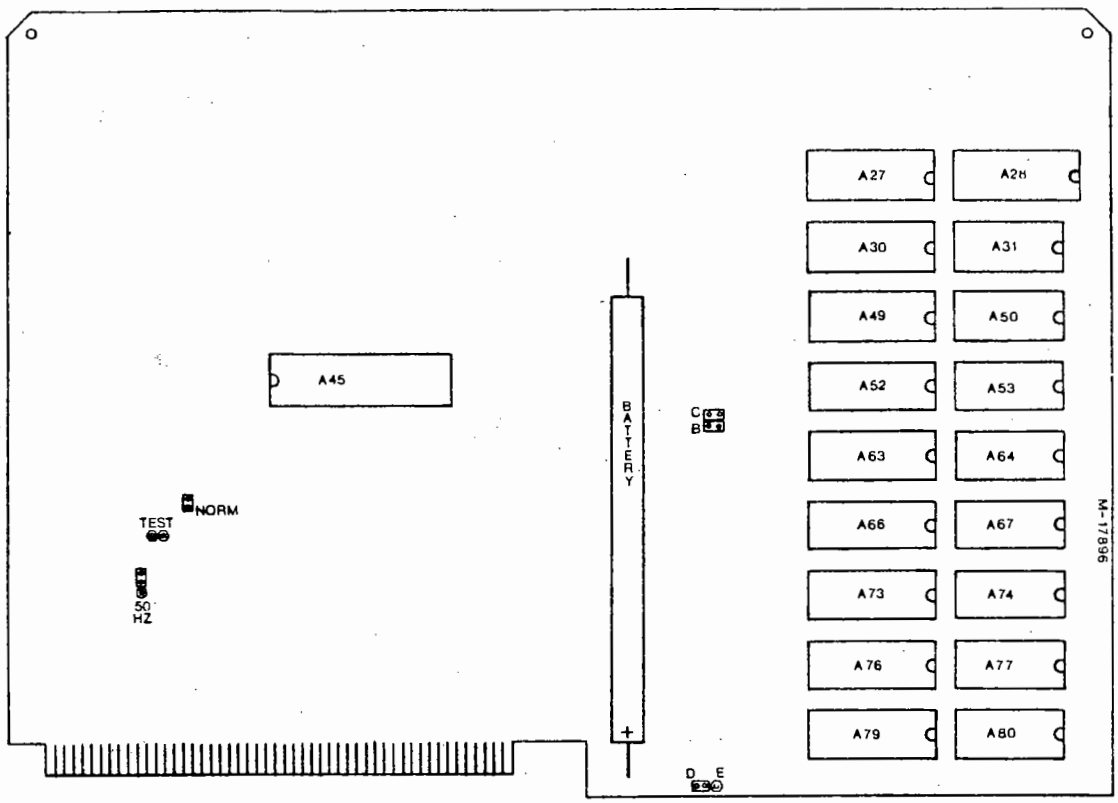


Figure A.2 CPU Board

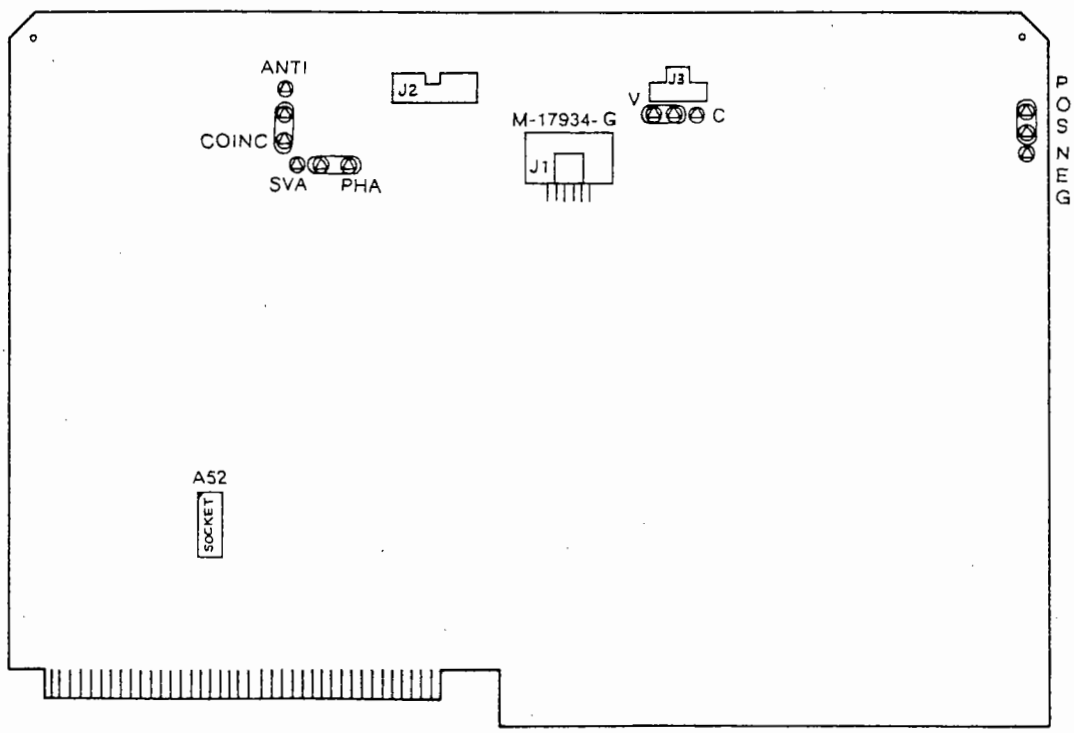


Figure A.3 ADC Board

V/C jumper to select the Voltage sensitive input mode or the Charge sensitive input mode. Shipped in the V position.

P/N jumper to select Positive inputs or Negative inputs in the Voltage sensitive mode only. Shipped in the Positive position.

A52 in the lower left corner of the board receives a plug for the Model 3531A Mixer/Router option. The plug, which is shipped with the option, is configured for a particular memory size; it must be used for that memory size only.

A.4 DISPLAY BOARD AND MONITOR

The only user control on the Display board is the Test Switch, S1, located at the rear of the top edge of the board. Depressing this switch will superimpose a test pattern, composed of rows of dots, on the screen. Its primary use is in checking the linearity of the monitor.

The switch may be locked in the test position by rotating it clockwise after it has been depressed. The switch must be restored to its normal, unlocked, position before proceeding with normal operation of the analyzer.

There is a connector on the monitor's CRT. Its pinout, from right to left when connected to the CRT, is:

Pin	Signal
1	+15 volt return and LSYNC return
6	LSYNC
7	+15 volt supply
8	VIDEO
9	FSYNC/
10	VIDEO return and FSYNC/ return

A.5 MISCELLANEOUS LOGIC BOARD (figure A.4)

C IN/C OUT jumper controls the transmission of control (CTL) characters to a peripheral device. CTL is used by the Series 35 PLUS during Readin. Some Readout-only devices will not accept CTL. The jumper is shipped in the C IN position, which enables transmission of CTL. If the peripheral device to be used with the Series 35 PLUS will not accept CTL, the jumper must be moved to the C OUT position. If a peripheral device is ordered from Canberra at the same time as the Series 35 PLUS, the jumper will be positioned correctly for that device.

Jumper A-B controls signal Ready. In the A position, DTR (Data Terminal Ready) generates Ready. Position B allows either DTR or RRDY (Receiver Buffer Empty) to generate Ready; used with faster EIA devices. Shipped in the A position.

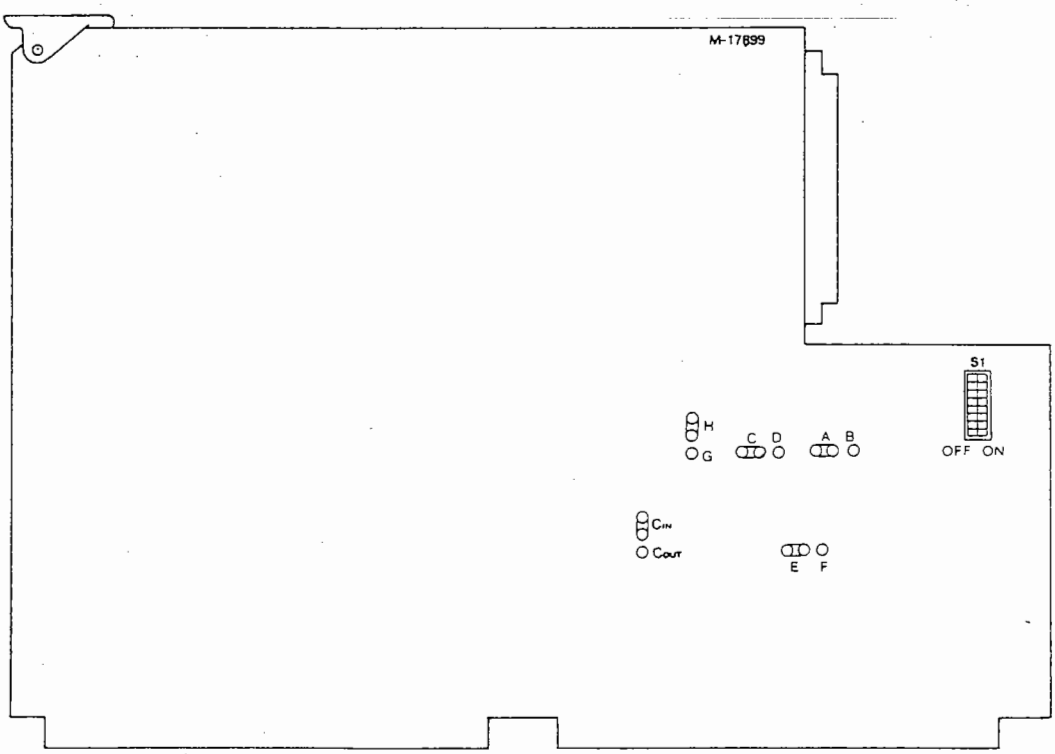


Figure A.4
Miscellaneous Logic Board

Jumper C-D controls signal Interrupt. In the C position, TXMT (Transmitter Buffer Empty) signals the USART Interrupt. In the D position TRDY (Transmitter Empty) signals the USART Interrupt; used with faster EIA devices. Shipped in the C position.

Jumper E-F controls the polarity of the BUSY flag, which is used to enable the Model 5421M Cassette Recorder's tape drive motor and to provide a Busy indication to an EIA device during Readin. Shipped in the E (negative true) position. If a positive true flag is required, the jumper must be changed to the F position.

Set the G-H jumper as follows:

G- For use with a Model 8222A or 8222B Mixer/Router WITHOUT the -01 Live Time Option, or for the Model 3523 Multi-ADC Interface.

H- For use with a Model 8222A or 8222B Mixer/Router WITH the -01 Live Time Option or for the Models 3524 External ADC Interface or 3521 Amp/ADC not using a Mixer/Router.

The DIPswitch, S1, controls several functions concerned with data I/O, as follows:

Shipped	Number	Function	On	Off
OFF	1-3	Set EIA rate	See table A.2	
ON	4	EIA rate	Variable	110 baud
ON	5	Parity select	Enable	Disable
ON	6	Parity	Even	Odd
ON	7	TTY rate	300 baud	110 baud
OFF	8	CAS/EIA	Cassette	EIA device

NOTE: Switches 7 and 8 can be set to the OFF position and, by grounding J101-pin 23 for switch 7 or J101-pin 18 for switch 8, can be remotely set to the ON position.

The Model 5421F Cassette Interface can be used for both the cassette and an EIA device. When the interface's TERMINAL/CASSETTE switch is moved "out", switch 8 will be remotely set to ON and the Analyzer will be set for cassette operation. Refer to the Model 5421 manual for details of operation.

Table A.2
Standard I/O Baud Selection

Baud Rate	Switch Numbers 1	2	3
300	OFF	OFF	OFF
600	ON	OFF	OFF
1200	OFF	ON	OFF
2400	ON	ON	OFF
4800	OFF	OFF	ON
9600	ON	OFF	ON

A.6 LOW VOLTAGE POWER SUPPLY

The Low Voltage Power Supply has five LED indicators at the top of the board which show that each supply is functioning. The indicators, from front to back, are:

+ 5 volts
-24 volts
+24 volts
+12 volts
-12 volts

Connector J1, also at the top of the board, has the following pinout:

Pin	Signal
1	ac to + 5 regulator
2	ac to + 5 regulator
3	ac return from + 5 regulator
4	ac return from + 5 regulator
5	ac return from ±12 and +15 regulators
8	+24 volts to preamp connector
11	preamp connector ground
12	HVPS connector ground
13	ac to ±24 regulator
14	ac to +5 regulator
15	ac return from +5 regulator
16	ac to ±12 and +15 regulators
17	ac to ±12 and +15 regulators
18	ac return from ±12 and +15 regulators
20	+24 to HVPS connector
21	-12 volts to preamp connector
22	+12 volts to preamp connector
23	-24 volts to preamp connector
24	ac return from ±24 regulator
25	ac return from +24 regulator

A.7 X-Y PLOTTER BOARD (figure A.5)

Control NABL is a factory set for low level true. To invert this level, change jumper B-C to B-A.

Control SEEK is factory set for high level true. To invert this level, change jumper E-F to E-D.

The pinout of the 25-pin connector at the top of the board is the same as the pinout of the X-Y Plotter connector (J107 or J108) on the analyzer's rear panel.

For line plotters that do not provide an Advance output, the plot rate can be adjusted from 2 to >10 channels per second with RV1. Line plotters without an external disable must have their servos turned OFF when not in the Plot mode.

Refer to section A.11.5 for rear panel connector signal list.

A.8 SERIAL INTERFACE BOARD (figure A.6)

The 52/53/73 jumper defines the use of this board; the jumper must be in the 52 position for use with the Model 3552A Printer/Plotter Interface, in the 53 position for use with the Model 3553 Graphics Plotter Interface or in the 73 position for use with the Model 3571 or 3573 Computer Interface.

The C-D jumper must be in the position specified in the option's operating instructions.

The H-I jumper must be in the H position for the Model 3571 or 3573 Computer Interface. Other options use the I position.

The M-N jumper has a unique function for the Models 3252A and 3253; it has no function for the Model 3571, 3573, and 3573B.

3252A: The M-N jumper enables transmission of control (CTL) characters.

N (or OUT) - CTL characters are transmitted.
M - inhibits CTL. For readout-only devices which will not accept control characters.

Refer to section A.11.5 for rear panel connector signal list.

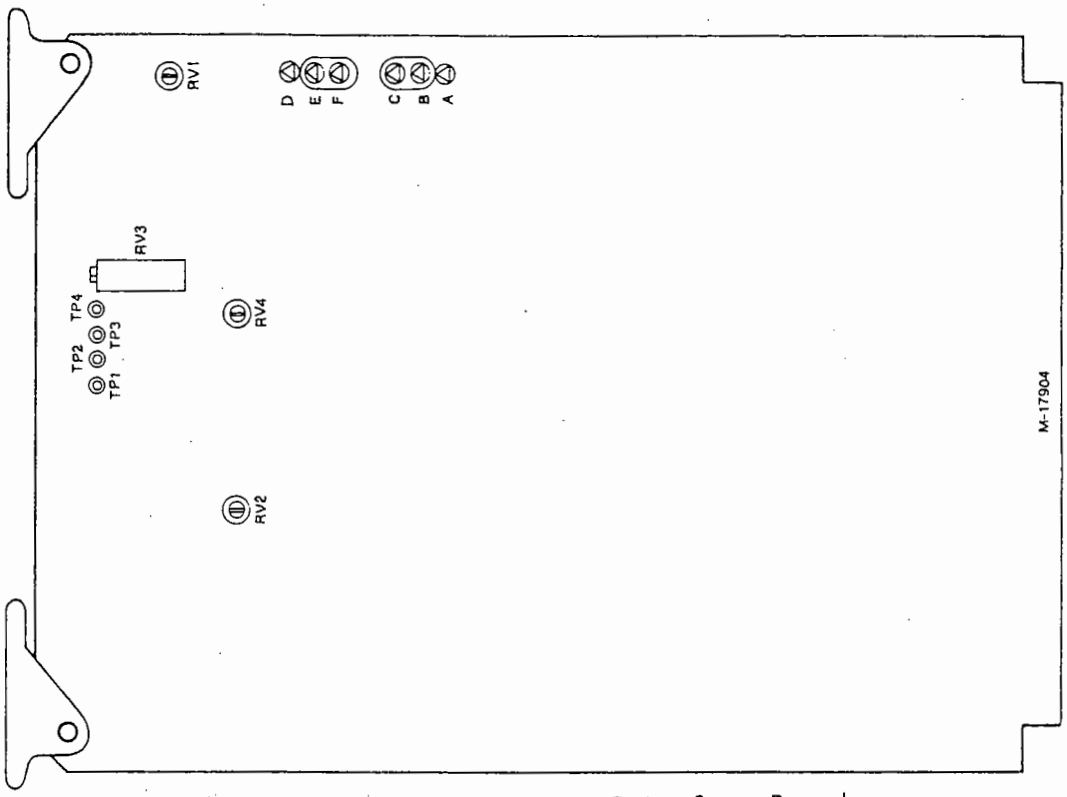


Figure A.5 X-Y Plotter Interface Board

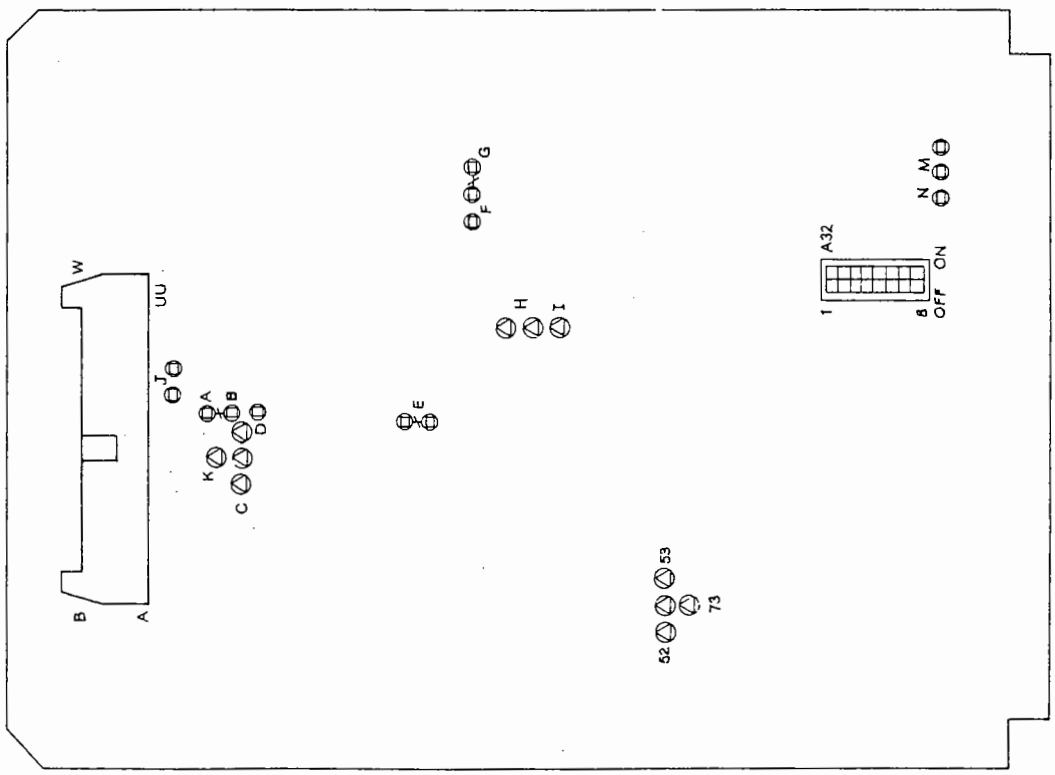


Figure A.6 Serial Interface Board

3553: the M-N jumper controls plot mode
N (or OUT) - line-plot mode is enabled.
M - point-plot mode is enabled.

3571, 3573, and 3573B: M-N jumper has no effect. The board is shipped with no M-N jumper installed.

The DIPswitch at the bottom of the board controls several functions as defined below:

Number	Function	On	Off
1-4	Set baud rate	See table A.3	
5	Word Length	7 Characters	8 Characters
6	Parity Select	Disables	Enables
7	Parity	Odd	Even
8	Stop Bits	One	Two

Table A.3
Serial I/O Baud Rate Selection

Baud Rate	Switch Numbers 1	2	3	4
75	OFF	ON	ON	ON
110	ON	OFF	ON	ON
134.5	OFF	OFF	ON	ON
150	ON	ON	OFF	ON
300	OFF	ON	OFF	ON
600	ON	OFF	OFF	ON
1200	OFF	OFF	OFF	ON
1800	ON	ON	ON	OFF
2000	OFF	ON	ON	OFF
2400	ON	OFF	ON	OFF
3600	OFF	OFF	ON	OFF
4800	ON	ON	OFF	OFF
7200	OFF	ON	OFF	OFF
9600	ON	OFF	OFF	OFF
19200	OFF	OFF	OFF	OFF

For the External Clock option (available by special order), set all switches to ON.

See the option's operating instructions for the correct switch settings.

The connector at the top of the board has the following pinout:

For RS 232 (Models 3552, 3553 3571 and 3573B)		For RS 422 (Model 3573)	
Pin	Signal	Pin	Signal
A	Ground	LL	Clear to send +
M	Data in	KK	Clear to send -
C	Data out	PP	Carrier detect +
L	RTS	RR	Carrier detect -
H	CTS	TT	Data set ready +
D	DSR	SS	Data set ready -
B	Ground	NN	Data out +
J	DCD	MM	Data out -
K	Flag	VV	Ground
N	DTR	UU	Ground
E	Busy	CC	Data in +
Z	422 In	DD	Data in -
X	Ground	FF	Data term ready +
Y	422 Out	EE	Data term ready -
W	Ground	HH	Request to send +
		JJ	Request to send -
		AA	Ground
		BB	Ground

A.9 MAGNETIC TAPE INTERFACE BOARD (figure A.7)

The ABC, DEF, and GHI jumpers define the data-block size. Factory set to 256 channels/block.

Block Size	Jumper Configuration		
note 1	B-C	E-F	H-I
256	A-B	E-F	H-I
512	B-C	D-E	H-I
1024	A-B	D-E	H-I
2048	B-C	E-F	G-H
4096	A-B	E-F	G-H
8192	B-C	D-E	G-H
note 2	A-B	D-E	G-H

Note 1: not valid; defaults to 256.
Note 2: not valid; defaults to 8192.

Refer to section A.11.5 for rear panel connector signal list.

The XYZ jumper allows the interface to record a time-of-readout Tag: a six-character Time-of-Day Code followed by a six-character Data Code at the start of each block. Factory set to disable the Tag Word.

Position	Tag Word
Y-Z	Disabled
X-Y	Enabled

The KLM jumper is set to K-L to enable communication between the interface and the Model 8531A Controller. The L-M position is not currently used.

The 2716/2732 jumper is set to 2716, the type of chip in socket A50. The 2732 position is not currently used.

Refer to section A.11.5 for rear panel connector signal list.

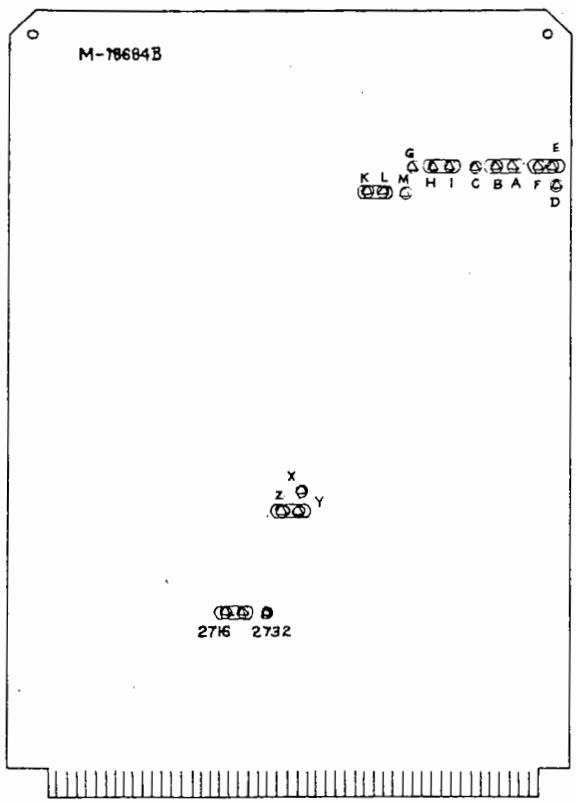


Figure A.7
Mag Tape Interface Board

A.10 GPIB INTERFACE BOARD (figure A.8)

The GPIB board has one jumper, which must always be in the B0 position, and an 8-pole rocker switch. Refer to the Model 3572 GPIB Interface manual for the switch settings.

Refer to Section A.11.5 for rear panel connector signal list.

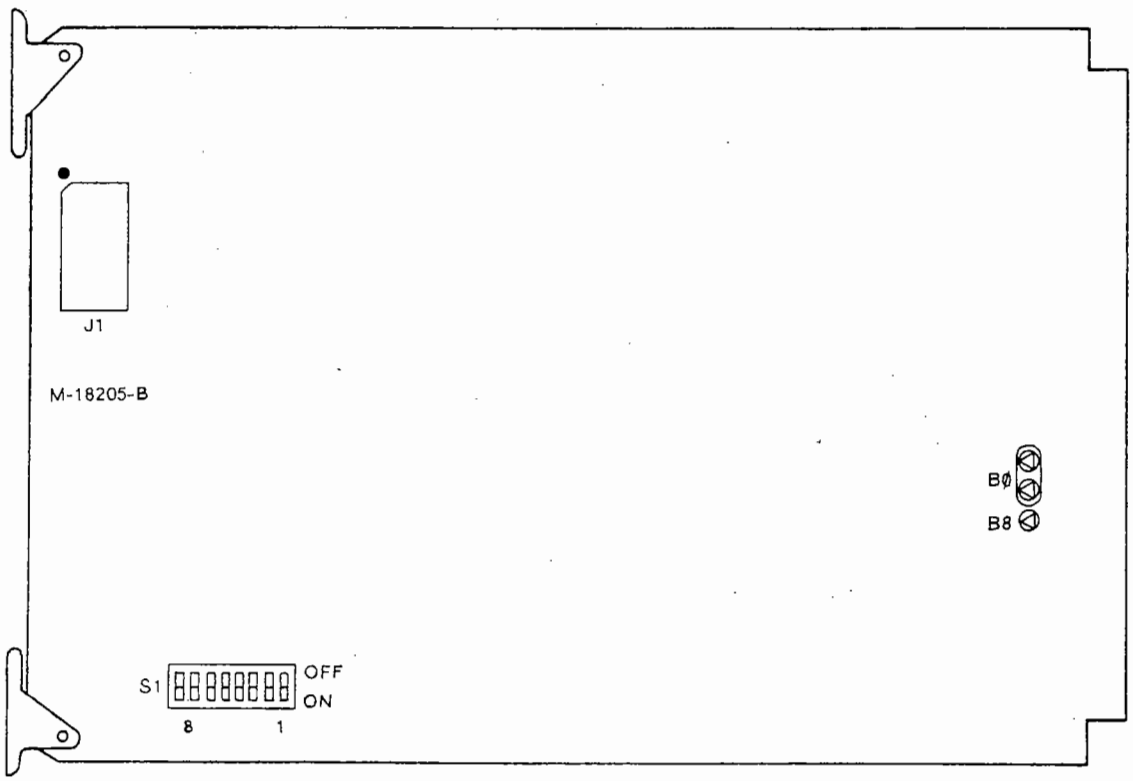


Figure A.8 GPIB Board

A.11 REAR PANEL CONNECTORS (figure B.4)

Jack#	Function	Connector Size
J101	EIA (RS232)	25 pin
J102	TTY	9 pin
J104	AC Power In	
J105	Mixer/Router	25 pin
J106	Stabilizer/External ADC	25 pin
J107	I/O Options (any 2 of following)	25 pin
J108	3551,-52,-53,-54,-71,-72,-73,-74	25 pin
J109	HVPS Power Enable	3 pin
J110	Preamp Power	9 pin
J111	MCS Count In	BNC
J112	Mössbauer/External Control	25 pin
J113	External ADC	25 pin
J114	External ADC	25 pin
J115	External ADC	25 pin
J116	Pileup Rejector	3 pin
J117	Pileup Rejector	BNC

Note 1: J116 and J117 are assembled on one plate; indentified "PUR"
Note 2: J111 and J112 are assembled on one plate; identified "REMOTE"
Note 3: The Model 3572 connector has 24 pins

A.11.1 J101 - EIA

Pin	Signal	Description
1	AA	Ground
2	BA	Received data (in from device)
3	BB	Transmitted data (out to device)
4	CA	Ready to send (in from device)
5	CB	Clear to send (out to device)
6	CC	Data set ready
7	AB	Ground
8	CF	Received line signal detector
9	--	+12V dc out
10	--	-12V dc out
11	--	Flag (in from device)
18	--	5421M external enable
20	CD	Data terminal ready
23	--	TTY baud select
25	--	Busy (to device)

A.11.2 J102 TTY Signals

Pin	Signal	Description
1	TTY Sol -	Motor Start Return
2	Tx +	Transmit
3	Gnd	Ground
4	TTY Sol +	Motor Start
6	Rx -	Receive Return
7	Rx +	Receive
9	Tx -	Transmit Return

A.11.3 J105 Mixer/Router Signals

Pin	Signal	Description	Direction Referred to Series 35+
1	EG3	Enable Group 3	Out
2	HIMR/	High Performance M/R	In
3	RA	Time Code Bit 0	In
4	MRAK/	Time Code Transfer Complete	Out
5	RB	Time Code Bit 1	In
6	EG4	Enable Group 4	Out
7	EG2	Enable Group 2	Out
8	IND/	Enable 16 Inputs	Out
9	2N-2	Routing Code Bit 0	In
10	2N-1	Routing Code Bit 1	In
11	2N	Routing Code Bit 2	In
12	2M	Routing Code Bit 3	In
13	INA/	Enable 2 Inputs	Out
14	TRMR/	ADC Conversion Complete	Out
15	CTM/	Clear Timers	Out
16	IA1/	Inhibit Add 1	In
17	TRMR/	ADC Conversion Complete	Out
18	EG1	Enable Group 1	Out
19	MRTT/	Time Tick Ready	In
20	GND	Ground	--
21	DT/	Dead Time	In
22	GND	Ground	--
23	INB	Enable 4 Inputs	Out
24	GND	Ground	--
25	INC/	Enable 8 Inputs	Out

Signal Levels
High (H) 2.4 to 5 V at <0.4 mA (2.4 V)
Low (L) 0.0 to 0.3 V at 2 mA

Mixer/Router Address Routing

The following chart is a truth table for the routing code bits (J105, pins 9, 10, 11, and 12). It also shows the relationship between the selected number of inputs and the memory segment where each input is stored.

Where
1 = >+3.0V
0 = <+0.3V
X = don't care

Inputs	Memory	2^M	2^N	2^{N-1}	2^{N-2}
1	Full	x	x	x	x
2	1/2	0	x	x	x
	2/2	1	x	x	x
4	1/4	0	0	x	x
	2/4	0	1	x	x
	3/4	1	0	x	x
	4/4	1	1	x	x
8	1/4	0	0	0	x
		0	0	1	x
	2/4	0	1	0	x
		0	1	1	x
	3/4	1	0	0	x
		1	0	1	x
	4/4	1	1	0	x
		1	1	1	x
16	1/4	0	0	0	0
		0	0	0	1
		0	0	1	0
		0	0	1	1
	2/4	0	1	0	0
		0	1	0	1
		0	1	1	0
		0	1	1	1
	3/4	1	0	0	0
		1	0	0	1
		1	0	1	0
		1	0	1	1
	4/4	1	1	0	0
		1	1	0	1
		1	1	1	0
		1	1	1	1

A.11.4 J106 Stabilizer Data/External ADC:

Pin	Signal	Description
1	SA2$_0$/	Gated Binary Address Data
2	SA2$_1$/	Gated Binary Address Data
3	SA2$_2$/	Gated Binary Address Data
4	SA2$_3$/	Gated Binary Address Data
5	SA2$_4$/	Gated Binary Address Data
6	SA2$_5$/	Gated Binary Address Data
7	SA2$_6$/	Gated Binary Address Data
8	SA2$_7$/	Gated Binary Address Data
9	SA2$_8$/	Gated Binary Address Data
10	SA2$_9$/	Gated Binary Address Data
11	SA2$_{10}$/	Gated Binary Address Data
12	SA2$_{11}$/	Gated Binary Address Data
13	SA2$_{12}$/	Gated Binary Address Data
14	ADCRDY/	ADC Ready
16	IA1/	Inhibit Add One
17	DACCP/	Data Accept
18	ENCOL	Enable Collect
20	STAB GAIN	Stabilizer Gain ($\pm$5 V)
21	STAB ZERO	Stabilizer Zero ($\pm$5 V)
22	ENDATA/	Enable Data
23	STAB TRIG	Stabilizer Trigger
24	GND	Ground

Note: When Model 3523 or 3524 is installed, J106 is defined as in A.11.9.

A.11.5 J107 and J108 I/O Connectors

These Connectors are used for any two of the following I/O Options (see note):

Model Number	Interface Type
3551	X-Y Point Plotter Interface
3552A	EIA Printer/Plotter Interface
3553	Graphics Plotter Interface
3554	Magnetic Tape Interface
3571	9.6 kbaud Computer Interface
3572	GPIB Interface
3573	19.2 kbaud Computer Interface

NOTE: Models 3551, 3552A, and 3553 are mutually exclusive. Models 3571, 3572, 3573, and 3573B are mutually exclusive.

Each connector is covered in detail on the following pages.

Model 3551 Connector

Pin	Signal	Description
2	XGND	X Ground
4	YGND	Y Ground
5	SEEK	Coordinate Control Out
6	CPC	Completed Plot Control In
9	NABL	Plotter Enable Out
14	GND	Ground
21	PLTY	Y Plot
23	PLTX	X Plot

Model 3552A/3553 Connector (RS232)

Pin	Signal	Description
1	GND	Ground
2	DATA IN	Received Data from device
3	DATA OUT	Transmitted Data to device
4	RTS	Ready to Send from device
5	CTS	Clear to Send to device
6	DSR	Data Set Ready
7	GND	Ground
8	DCD	Received Line Signal Detect
11	FLAG	Flag from device
20	DTR	Data Terminal Ready
25	BUSY	Busy to device

Pin 11: a TTL or RS232 low level input from the device stops data output after the current character. A high level signals device Ready.

Model 3554 Connector

Pin	Signal	Direction referred to Series 35 PLUS
1	WD1/	Out
2	WDO/	Out
3	WD2/	Out
4	WD3/	Out
5	GND	--
6	GND	--
7	RD3/	In
8	RD2/	In
9	GND	--
10	RD1/	In
11	RDO/	In
12	BCD/	Out
13	RI/	Out
14	ESPI/	Out
15	RO/	Out
16	ADDRESS/	Out
17	MT/	Out
18	ADRNO/	In
19	I/O ATX/	In
20	GAP/	In
21	SP/	In

Model 3571 Connector (RS232)

Pin	Signal	Direction referred to Series 35 PLUS
1	Ground	---
2	Data In	In
3	Data Out	Out
4	Request to Send (RTS)	In
5	Clear to Send (CTS)	Out
6	Data Set Ready (DSR)	Out
7	Ground	---
8	Carrier Detect (CD)	Out
11[1]	Flag	In

1. Active input normally on Pin 11. Internal jumper to use pin 4.

Model 3572
GPIB Connector

Pin	Signal	Description
1	DIO1	Data I/O 1
2	DIO2	Data I/O 2
3	DIO3	Data I/O 3
4	DIO4	Data I/O 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready for Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	To Earth Ground
13	DIO5	Data I/O 5
14	DIO6	Data I/O 6
15	DIO7	Data I/O 7
16	DIO8	Data I/O 8
17	REN	Remote Enable
18	Twisted Pair with pin 6	
19	Twisted Pair with pin 7	
20	Twisted Pair with pin 8	
21	Twisted Pair with pin 9	
22	Twisted Pair with pin 10	
23	Twisted Pair with pin 11	
24	GND	Signal Ground

Model 3573 Connector
(RS422)

Pin	Signal	Direction referred to Series 35 PLUS
1	GND	---
3	Received Data +	In
6	Request to Send +	In
8	Clear to Send -	Out
10	Data Set Ready +	Out
11	Terminal Ready +	In
12	Carrier Detect +	Out
13	GND	---
14	GND	---
15	Received Data -	In
17	Transmitted Data -	Out
18	Request to Send -	In
20	Clear to Send +	Out
22	Data Set Ready -	Out
23	Terminal Ready -	In
24	Carrier Detect -	Out
25	GND	---

Model 3573B Connector (RS232)

Pin	Signal	Direction referred to Series 35 PLUS
1	Ground	---
2	Data In	In
3	Data Out	Out
4[1]	Request to Send (RTS)	In
5	Clear to Send (CTS)	Out
6	Data Set Ready (DSR)	Out
7	Ground	---
8	Carrier Detect (CD)	Out
11	Flag	In
20	Data Terminal Ready (DTR)	In
25[2]	Busy	Out

1. Active input normally on pin 4. Internal jumper to use pin 11.

2. No function in this interface.

A.11.6 J109 High Voltage Power Supply Connector

Pin	Signal	Description
1	GND	Ground
2	+24 V	+24 volt dc supply
3	---	No connection

A.11.7 J110-Preamp Power Connector

Pin	Signal	Description
1	GND	Ground
2	GND	Clean Ground
4	+12 V	+12 volt dc supply
6	-24 V	-24 volt dc supply
7	+24 V	+24 volt dc supply
9	-12 V	-12 volt dc supply

A.11.8 J111 and J112 External Control/ Mössbauer Connector

Pin	Signal	Description
J111-BNC	COUNT	MCS Count Input (Model 3522)
J112:		
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	EXT ADV	MCS External Advance In
5	EXT TRIG	MCS External Trigger In
6	SCADV	Sample Changer Advance Out
7	BSYOUT/	MCA Busy Out
8	BSYIN	Device Busy In
9	COLLECT/	Status Out
10	I/O/	Status Out
11	STOPCOL/	Stop Collect In
12	STARTCOL/	Start Collect In
13	CLRDAT/	Clear Data In
14	AADV/	Address Advance Out
15	GATE	Gate In
16	SWOUT	Sweep Out
17	$SA2^9$/	Gated Binary Address Data
18	$SA2^{10}$/	Gated Binary Address Data
19	$SA2^{11}$/	Gated Binary Address Data
20	$SA2^{12}$/	Gated Binary Address Data
21	AMS	Abort MCS Sweep In
22	AOF	MCS Address Overflow Out
23	CIR	Count in ROI
24	CIAR	Count in Area ROI
25	STARTIO/	Start Readout In

A.11.9 J106, J113, J114, J115– External ADC Connectors

Chassis connectors (J106, J113, J114, J115): female 25-pin; Amphenol type 17-10250. J106 is used for the fourth external ADC.

Logic levels:
Logic High = +2.4 to +5 V
Logic Low = 0.0 to +0.3 V

Pin	Signal	Description
1	2^0/	
2	2^1/	
3	2^2/	
4	2^3/	
5	2^4/	ADC Address input:
6	2^5/	Logic 1 = low; 2^0 to 2^{11}
7	2^6/	require positive drive.
8	2^7/	2^{12} has a pull-up
9	2^8/	resistor on its input for
10	2^9/	use with 12-bit ADCs.
11	2^{10}/	
12	2^{11}/	
13	2^{12}/	
14	RDY/	ADC Converversion Ready input; Logic 1 = low; open circuit = Logic 0.
16	INHAD/	Inhibit Storage of Current Conversion input; Logic 1 = low; open circuit = Logic 0.
17	DAC/	Data Accepted output; 0.5 µs pulse; Logic 1 = low
21	DT	ADC Dead Time input; Logic 1 = high; open circuit = Logic 0.
22	ENDATA/	Enable ADC Address output; Logic 1 = low.
24	GND	Ground

A.11.10 NIM Slot

This Rear Panel Connector provides dc power to the following modules:

3100-01	Detector Bias Supply
3100-02	Spectroscopy Amplifier
4225	Spectroscopy Amplifier
8222B	Mixer/Router

No other modules may be installed in this connector.

A.11.11 J116, J117-PUR/LTC Connectors

Pin		Signal	Description
J116	1	LG/	Linear Gate Out
	2	REJ	Reject In
	3	GND	Ground
J117	BNC	ADC BUSY/	Busy In

APPENDIX B
FIELD INSTALLATION INSTRUCTIONS

B.1 INTRODUCTION

The Monitor (CRT Assembly) and individual boards can be removed or replaced by following the instructions included in this Appendix. Also included are detailed Field Installation instructions for options purchased later.

B.1.1 Cover Removal

Before removing the covers, turn off the ac power and remove the ac line cord from the rear of the Analyzer.

To remove the top and bottom covers, simply remove the four (4) black Phillips-head screws from each side of the covers, lift off the top cover, and lift the Analyzer out of the bottom cover. After replacing a board or installing an option, reconnect the ac line cord to the Analyzer, turn on the ac power and check the operation of the unit before replacing the covers.

If any question arises during the installation or the operational check-out, please contact your local Canberra Representative or Canberra's Customer Service Department.

B.1.2 Board Removal and Replacement

The Printed Circuit (PC) Boards may be removed from the Analyzer by applying equal pressure to the card ejectors at each end of the board and pulling up.

The boards are installed by aligning the board in the card guide slots mounted on the front and back of the card cage and sliding the board all the way down. Press the board firmly down into the Mother Board socket, flexing the board if necessary to align it with the socket. Be sure the board is firmly seated in the Mother Board socket.

The cable entry opening shown at the rear of the Monitor compartment (see figure B.1) is used to pass the wiring of various options from the rear panel connectors to the Mother Board edge connectors.

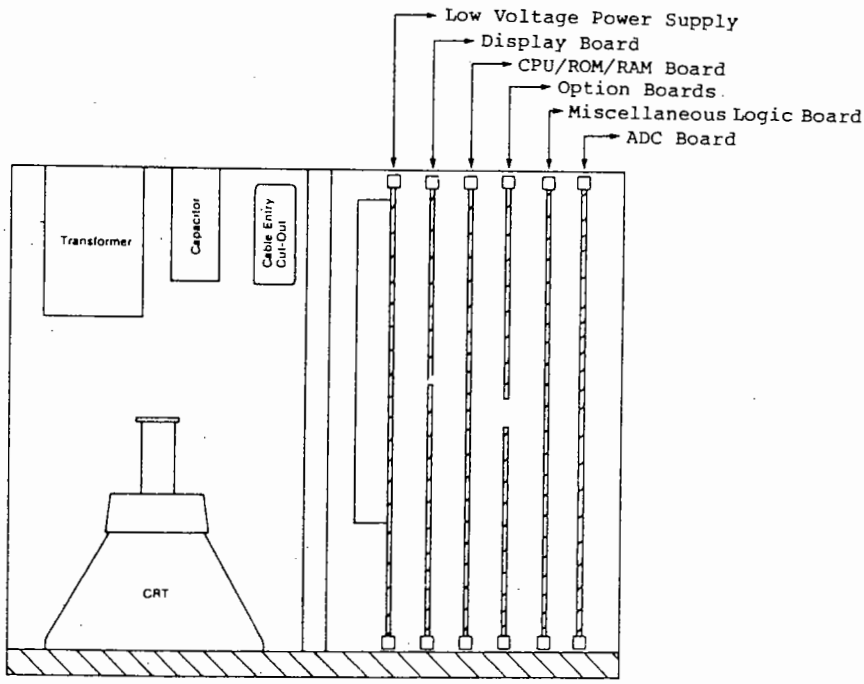


Figure B.1
Series 35 PLUS
Board Locations

B.1.3 Firmware Update

To change the basic Firmware set to a later version, all programmable chips, including any option chips, must be updated to the same Firmware revision level to allow proper operation of the Analyzer. Programmable chips are indicated by a label naming chip location and Firmware revision level.

To install the firmware:

1. Remove the CPU Board from the Analyzer.
2. Using a small screwdriver or an LSI chip-puller, carefully remove the programmable chips.
3. Insert the chips of the new Firmware set into the socket named on each chip's label.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board. The socket has a notch at this side as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

4. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
5. Before replacing the covers, check the installation for proper operation.
6. On power up, check Firmware version number displayed (see figure B.2) to verify that the correct Firmware set has been installed.

   Note: In an Analyzer with a Model 3571, 3572, or 3573 interface, the display of figure B.2 will not be seen at power on if the rear panel control switch is in the REMOTE position.

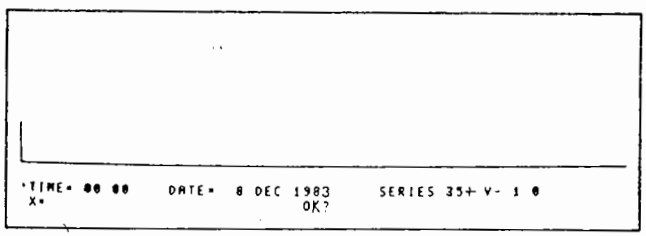


Figure B.2
Display at
Power On

B.1.4 Monitor Replacement

The Monitor Assembly can be removed by pulling the connector off of the rear of the Monitor Assembly printed circuit board and removing the four (4) screws, one in each corner of the bottom of the Monitor frame. A Phillips screwdriver with a 23 cm (9 in.) shank will make removal of the screws easier.

The Model 3562 Service Kit includes the 23 cm Phillips screwdriver and other useful servicing aids.

Pull the Monitor slightly to the rear and carefully lift it straight up and out of the Analyzer.

To reinstall the Monitor, reverse the removal procedure. Be sure that the wiring connector is seated securely on the printed circuit board edge connector and the four (4) screws are tightened down.

B.1.5 Field Installation of Options

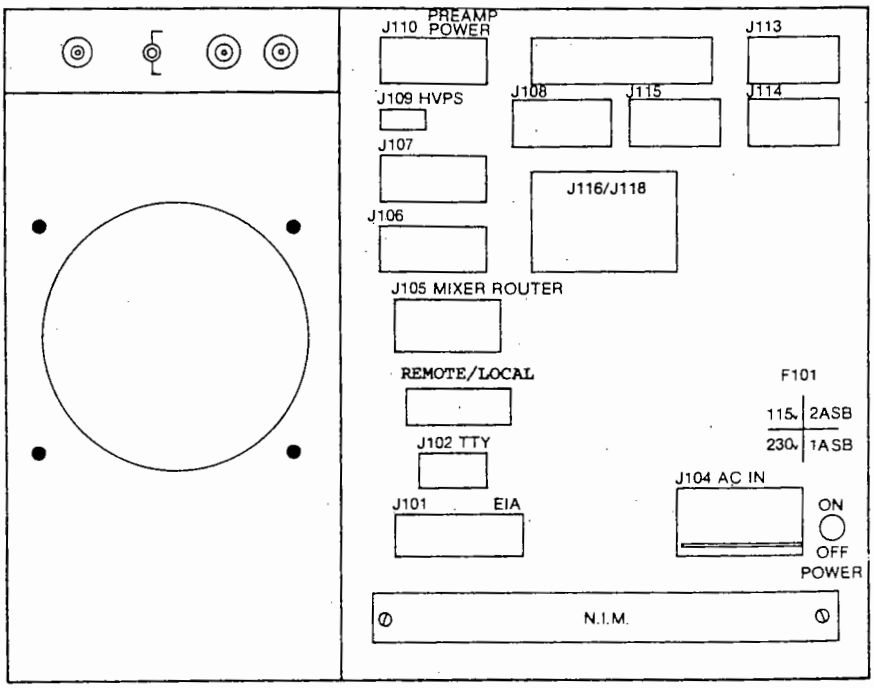
After removing the covers (see section B.1.1), proceed to the appropriate section of the manual for the option being installed.

After installing the option, move jumper D-E on the CPU board to the E position, let it stay there for about one minute, then move it back to D. This allows the system to recognize the presence of the option when the power is turned on.

Before replacing the covers, check the installation for proper operation.

When installing options that have a D-type male connector to be mounted on the Analyzer's rear panel, be sure to mount the connector narrow side down. Refer to figure B.3.

Figure B.3
Connector Orientation



Location	Designation
J101.....	EIA Connector
J102.....	Teletype Connector
J104.....	AC Line Input
J105.....	Mixer Router
J106.....	Stabilizer Data/External ADC 1
J107/J108.....	I/O Options
J109.....	High Voltage Power Supply
J110.....	Preamplifier Power Supply
J111/J112.....	MCS/Moessbauer/Ext. Control
J113/J114/J115..	External ADC 2,3,and 4
J116/J118.....	Pile-up Rejector

Figure B.4 Series 35 PLUS Rear Panel

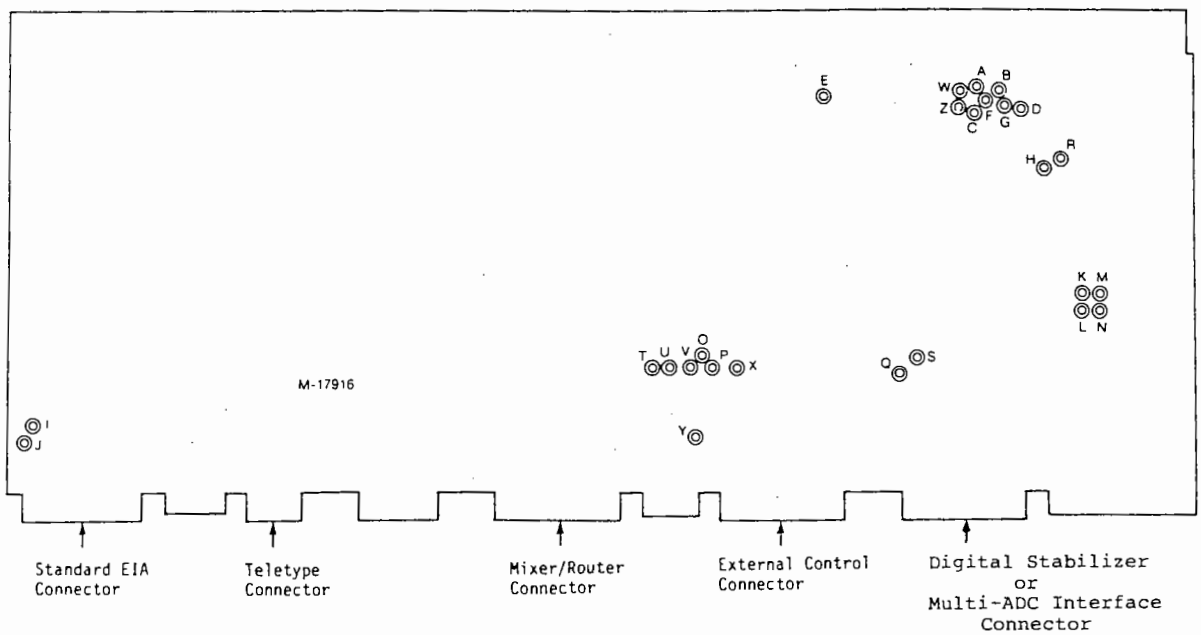


Figure B.5 Mother Board -- Bottom View

B.2 MODEL 3522 HIGH-PERFORMANCE MCS OPTION

The Model 3522 High Performance MCS option consists of a small plug-in printed circuit (PC) board. To install it:

1. Remove the Miscellaneous Logic Board from the Analyzer.
2. Plug the small PC board into J1, the connector at the top right corner of the Miscellaneous Logic Board.
3. Replace the board in the Analyzer.
4. Remove the CPU Board from the Analyzer. Move its D-E jumper to the E position for about one minute, then move it back to D. Replace the CPU Board in the Analyzer.
5. Before replacing the Analyzer's covers, check the installation for proper operation.

B.3 MODEL 3523 MULTI-ADC INTERFACE

The Model 3523 Multi-ADC Interface consists of the interface board with three (3) ribbon cables attached to it and a single separate ribbon cable.

Before installing the Interface Board, be sure that the jumpers are set correctly (figure B.6):

ANTI-COINC - Refer to section 10.3.3.
A-B - Used for testing only. Leave in the B position.
MUX-EXT ADC - Set to MUX position.

To install the interface:

1. Remove the cover plates from the Analyzer's rear panel, which are marked J113, J114, J115, and J106 (see figure B.4).
2. Remove the cables from J1, J2, and J3 on the Model 3521 ADC Board.
3. Remove the 3521 ADC Board from the Analyzer and replace it with the Model 3523 Interface.
4. Install the three attached ribbon cables, as marked, in J113, J114, and J115.
5. Install the separate ribbon cable in J106.
6. Fasten the connectors in place with the hardware supplied with the option.
7. Dress the three ribbon cables attached to the board across the back of the boards and place any cable slack inside the Monitor compartment.

9. Route the single separate ribbon cable (from J106) through the cable entry opening at the bottom right rear of the Monitor compartment.
10. Connect the three cables removed from the 3521 ADC Board to the mating connectors on the 3523 Interface Board.
11. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket.
12. Plug the cable's plastic connector onto the Mother Board's rear-most (Stabilizer) edge connector with the blue stripe on the cable to the right (see figure B.5).
13. Reinstall the cable retaining bracket and its three nuts.
14. Turn the Analyzer right side up and remove the Miscellaneous Logic Board.
15. Change jumper "H" to position "G" on the Miscellaneous Logic Board (see figure B.7).
16. Remove the CPU Board from the Analyzer. Move its D-E jumper to the E position for about one minute, then move it back to D. Replace the CPU Board in the Analyzer.
17. Before replacing the covers on the Analyzer, check the installation for proper operation.

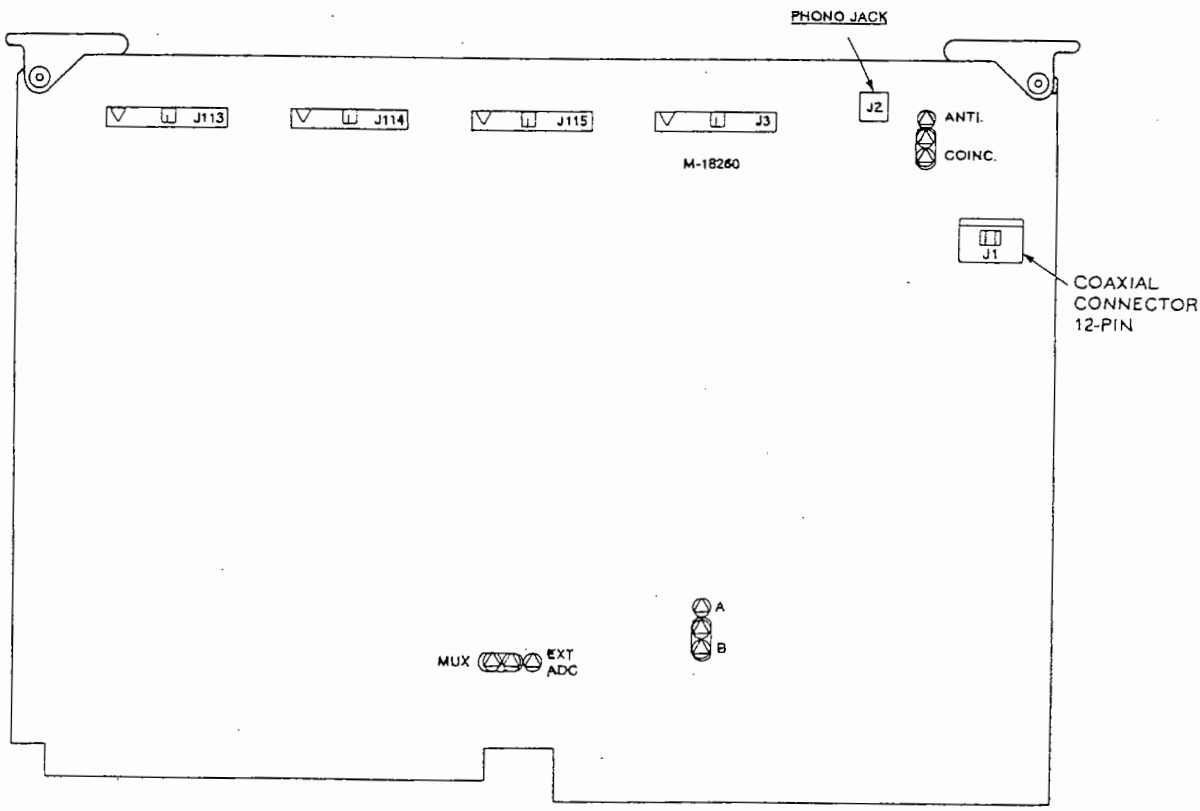


Figure B.6 ADC Interface Board

B.4 MODEL 3524 EXTERNAL ADC INTERFACE

The Model 3524 External ADC Interface consists of an interface board and a ribbon cable.

Before installing the Interface Board, be sure that the jumpers are set correctly (see figure B.6):

ANTI-COINC - Refer to section 10.4.3.
A-B - Used for testing only. Leave in the B position.
MUX-EXT ADC - Set to EXT ADC position.

To install the interface:

1. Remove the cover plate from the Analyzer's rear panel labeled J106.
2. Remove cables J1, J2 and J3 from the Model 3521 ADC board.
3. Remove the 3521 ADC board from the Analyzer.
4. Insert the 3524 board in its place.
5. Connect J1, J2, and J3 (removed from the 3521 ADC Board) to the mating connectors on the Interface board.
6. Install the ribbon cable in J106.
7. Fasten the connector in place with the hardware supplied with the option.
8. Carefully route the ribbon cable from J106 through the cable entry opening at the bottom right rear of the Monitor compartment.
9. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket.
10. Plug the plastic connector on the cable from J106 into the rear-most edge connector, marked Stabilizer, of the Mother Board (see figure B.5) with the blue stripe on the cable to the right.
11. Reinstall the cable retaining bracket and its three nuts.
12. Turn the Analyzer right side up and remove the Miscellaneous Logic Board.
13. Set the Miscellaneous Logic Board jumper G-H to the "H" position (see figure B.7).
14. Remove the CPU Board from the Analyzer. Move its D-E jumper to the E position for about one minute, then move it back to D. Replace the CPU Board in the Analyzer.
15. Before replacing the covers on the Analyzer, check the installation for proper operation.

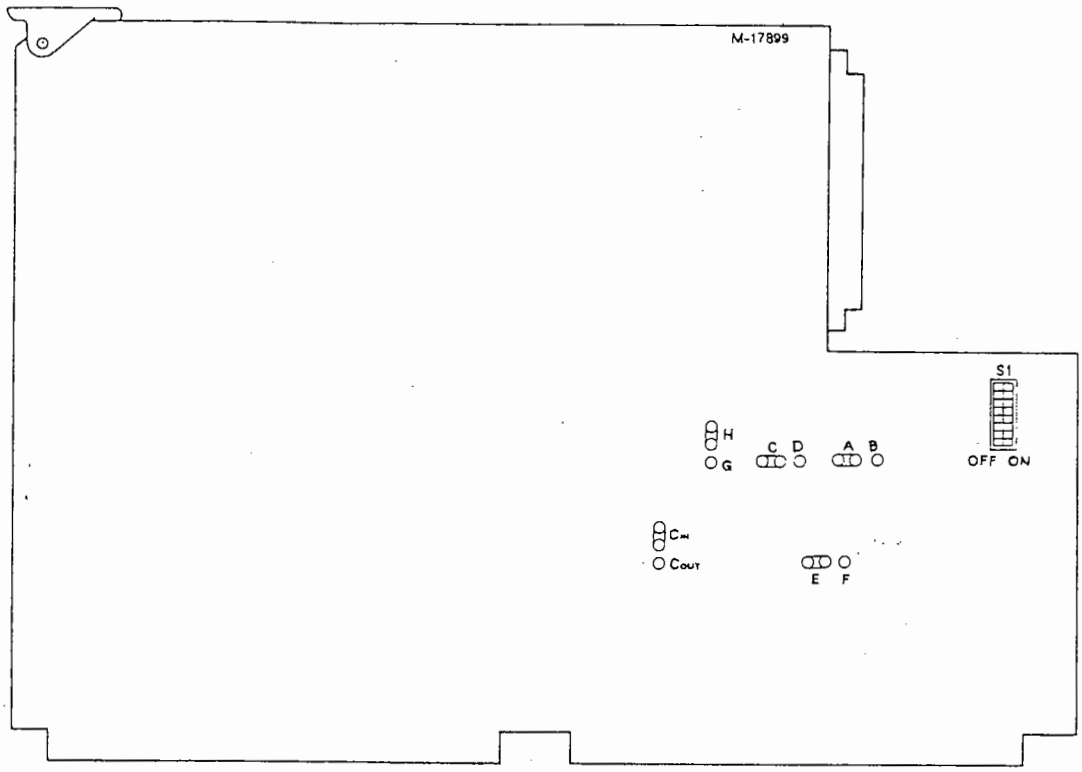


Figure B.7 Miscellaneous Logic Board

B.5 MODEL 3531A MIXER/ ROUTER WIRING

The Model 3531A Wiring option consists of a ribbon cable with a 25-pin, D-type connector at one end and a plastic edge connector at the other end, and three DIP jumper plugs.

1. Remove the cover plate on the Analyzer's rear panel, marked J105 (see figure B.4).
2. Mount the Model 3531A connector in the J105 opening and fasten it in place with the hardware supplied with the option.
3. Carefully route the ribbon cable through the cable entry opening at the bottom right rear of the Monitor compartment (see figure B.1).

4. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket.
5. Plug the plastic connector into the Mixer/Router edge connector on the Mother Board (see figure B.5) with the blue stripe on the cable to the right.
6. Reinstall the cable retaining bracket and its three nuts.
7. Turn the Analyzer right side up, remove the three cables at J1, J2, and J3 on the ADC Board and remove the ADC Board from the Analyzer.
8. Install one of the DIP jumper plugs in A52 on the ADC Board (see figure B.8). The plug used must match the Analyzer's memory size.

For Model:	Use the plug marked:
3501	High Perf. 2K
3502	High Perf. 4K
3503	High Perf. 8K

Be sure to insert the plug with the pin 1 marking at the top of the socket. Take care to ensure that no plug pins are left outside of the socket or bent under the plug.

9. Replace the ADC Board in the Analyzer and reconnect the three cables to J1, J2, and J3 on the ADC Board.
10. Remove the Miscellaneous Logic Board from the Analyzer and set its G-H jumper as follows: (See figure B.7).
    - G- For use with a Model 8222A or 8222B Mixer/Router WITHOUT the -01 Live Time Option, or for the Model 3523 Multi-ADC Interface.
    - H- For use with a Model 8222A or 8222B Mixer/Router WITH the -01 Live Time Option or for the Models 3524 External ADC Interface or 3521 Amp/ADC not using a Mixer/Router.
11. Remove the CPU Board from the Analyzer. Move its D-E jumper to the E position for about one minute, then move it back to D. Replace the CPU Board in the Analyzer.

Note: To use the Series 35 PLUS with an 8220A Mixer/Router, consult factory.

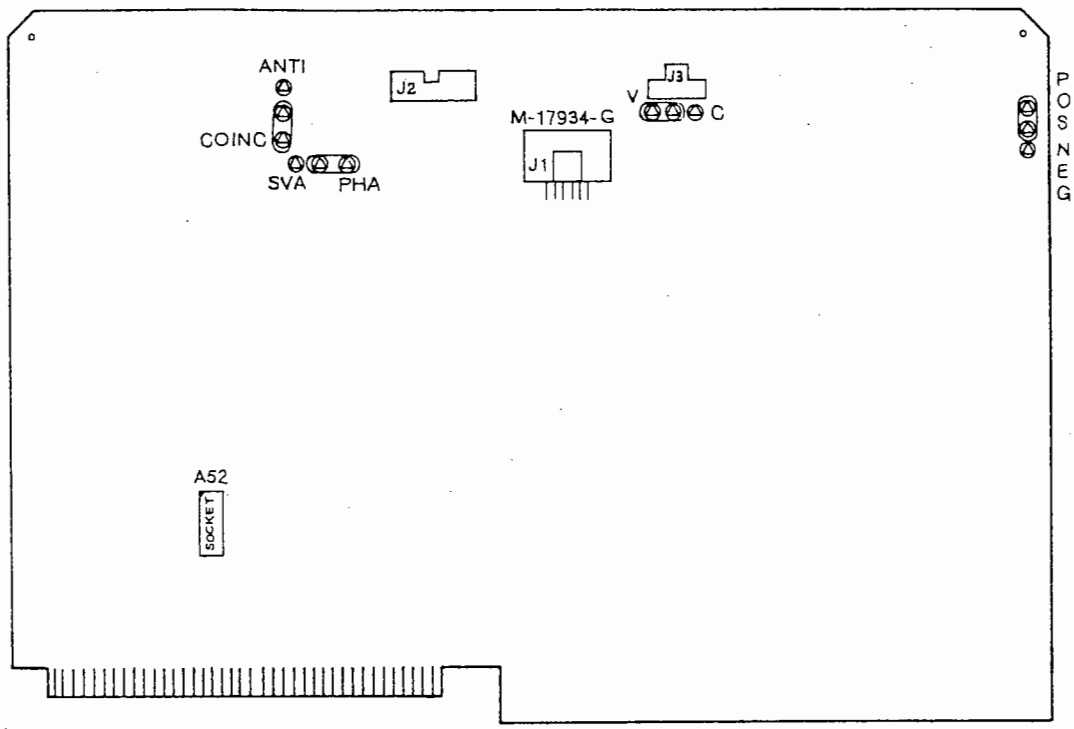


Figure B.8 ADC Board

B.6 MODEL 3533 DIGITAL STABILIZER WIRING

The Model 3533 Digital Stabilizer Wiring option consists of a ribbon cable with a 25-pin D-type connector at one end and a plastic edge connector at the other end.

1. Remove the cover plate on the Analyzer's rear panel marked J106 (see figure B.4).
2. Mount the Model 3533 connector in the J106 opening and fasten it in place with the hardware supplied with the option.
3. Carefully route the ribbon cable through the cable entry opening at the bottom right rear of the Monitor compartment.
4. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket.

5. Plug the plastic connector onto the Stabilizer edge connector on the Mother Board (see figure B.5) with the blue stripe on the cable to the right.
6. Replace the cable retaining bracket and its three nuts.
7. Turn the Analyzer right side up and connect the Model 8200 Stabilizer to J106 with the 25-pin cable supplied with the Stabilizer.

NOTE: Early Stabilizers used a 24-pin connector which will require an adapter cable.

An adapter cable may be ordered from the factory, assembled and tested, or may be made in the field by referring to section A.11.4 of this Manual.

8. Remove the CPU Board from the Analyzer. Move its D-E jumper to the E position for about one minute, then move it back to D. Replace the CPU Board in the Analyzer.
9. Before replacing the covers, check the installation for proper operation. Refer to the Stabilizer's Operators Manual for instructions on its operation.

B.7 MODEL 3541/3541C/3541N DEFINE/USE/AP-PAK

The Model 3541, 3541C or 3541N Define/Use/Ap-Pak option consists of three programmed integrated circuit chips. The chips are labeled with the Model number, the Firmware version, and a socket number.

The Firmware version number on the chips must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

To install the option:

1. Remove the CPU Board from the Analyzer.
2. Locate the socket number indicated on each chip (see figure B.9 for location).

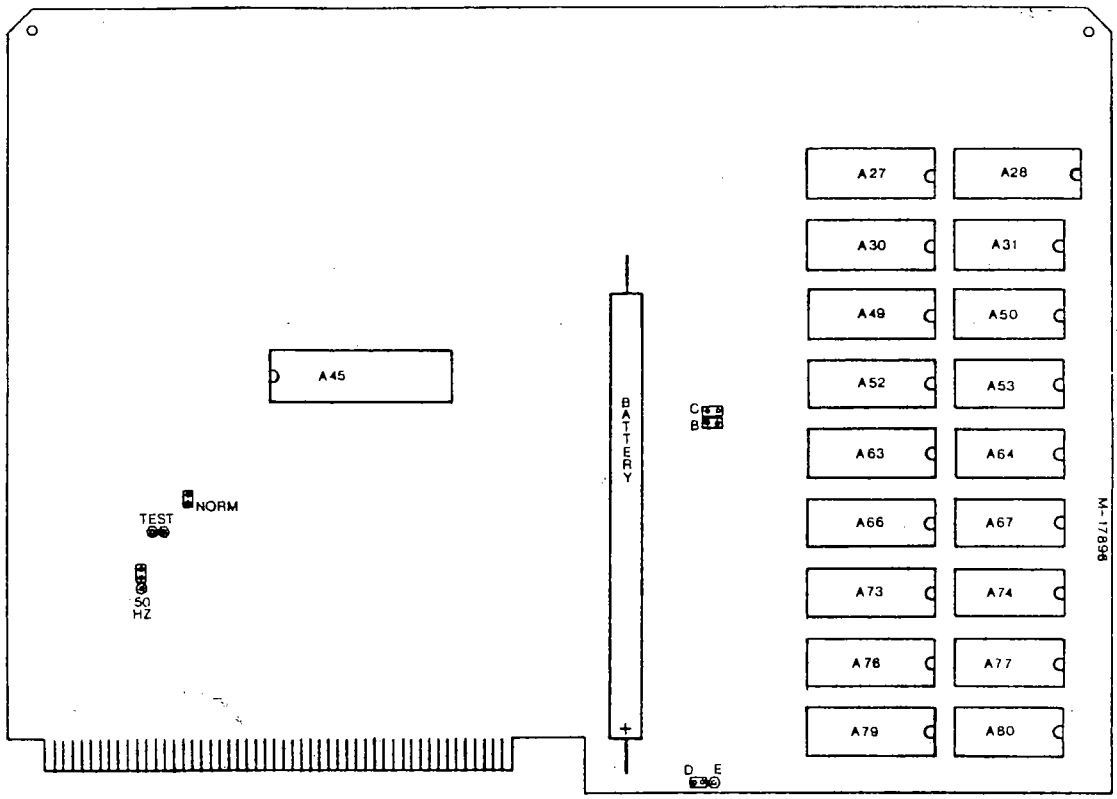
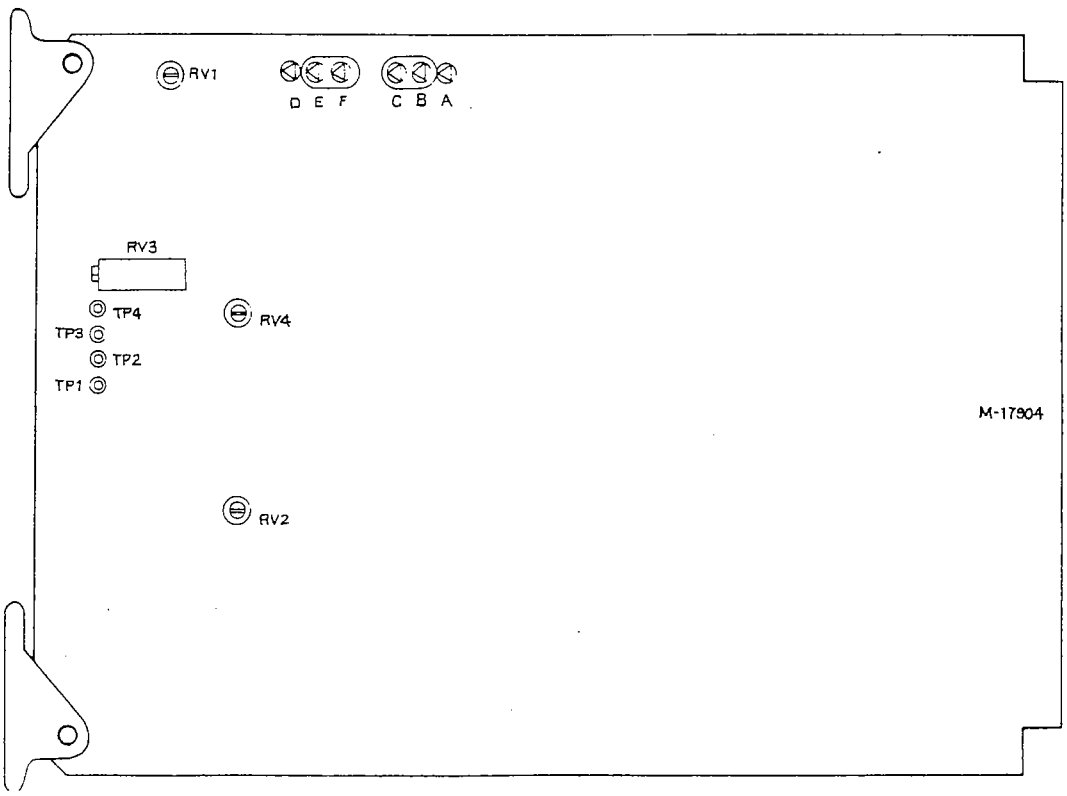


Figure B.9 CPU Board



3. Install the chips in the correct CPU Board sockets.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that each chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

4. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
5. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.8 MODEL 3543 ISOTOPE ANALYSIS

The Model 3543 Isotope Analysis option consists of two programmed integrated circuit chips. The chips are labeled with the Model number, the Firmware version, and the socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

To install the option:

1. Remove the CPU Board from the Analyzer.
2. Locate the socket numbers indicated on the chips (see figure B.9 for location).

3. Install the chips in the correct CPU Board sockets.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

4. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
5. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.9 MODEL 3544 X-RAY ELEMENTAL ANALYSIS

The Model 3544 X-ray Elemental Analysis option consists of two programmed integrated circuit chips and a modified Miscellaneous Logic Board. The chips are labeled with the Model number, the Firmware version, and the socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

To install the option:

1. Remove the CPU Board from the Analyzer.
2. Locate the socket numbers indicated on the chips (see figure B.9 for location).
3. Install the chips in the correct CPU Board sockets.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

4. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
5. Remove the existing Miscellaneous Logic Board from the Analyzer and replace it with the modified Miscellaneous Logic Board supplied with the option.
6. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.10 MODEL 3551 X-Y PLOTTER INTERFACE

The Models 3551, 3552A, and 3553 are mutually exclusive. Only one of these may be installed in the Analyzer.

The Model 3551 X-Y Plotter Interface consists of: a printed circuit board with an attached cable terminated in a connector; an identifying decal; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number. The interconnecting cable is attached to the Plotter.

The Firmware version number on the chip must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2).

If the two Firmware versions do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check the two jumpers on the board to verify that they are in positions B-C and E-F (see figure B.10). Refer to Appendix A.7 for jumper functions.

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see figure B.1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the Interface.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer.
8. Locate the socket number indicated on the chip (see figure B.9 for locations).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.11 MODEL 3552A PRINTER/ PLOTTER INTERFACE

Models 3551, 3552A, and 3553 are mutually exclusive. Only one of these may be installed in the Analyzer.

The Model 3552A Printer/Plotter Interface consists of a printed circuit board with an attached cable terminated in a 25-pin connector, an identifying decal, and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly. Refer to figure B.11.

52/53/73 jumper in the 52 position
C-D jumper in the D position
H-I jumper in the I position

With the M-N jumper out or in the N position, control characters (CTL) will be transmitted with the data. With a jumper in the M position, CTL will be inhibited.

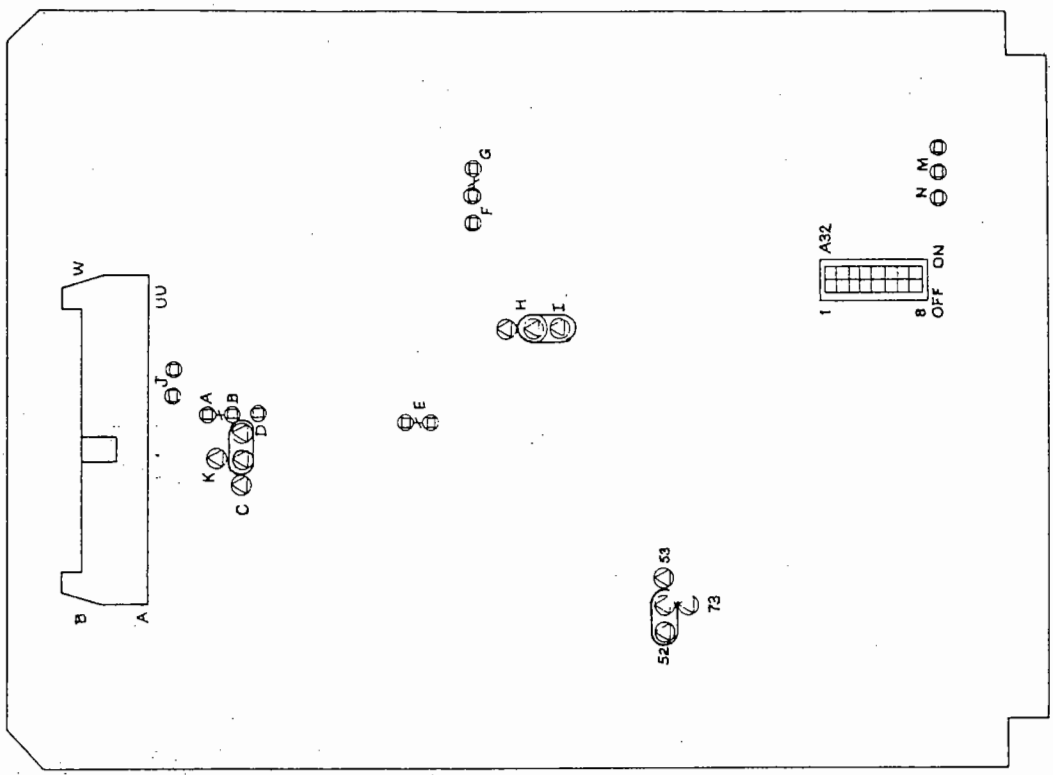


Figure B.11 Model 3552A Printer/Plotter Interface

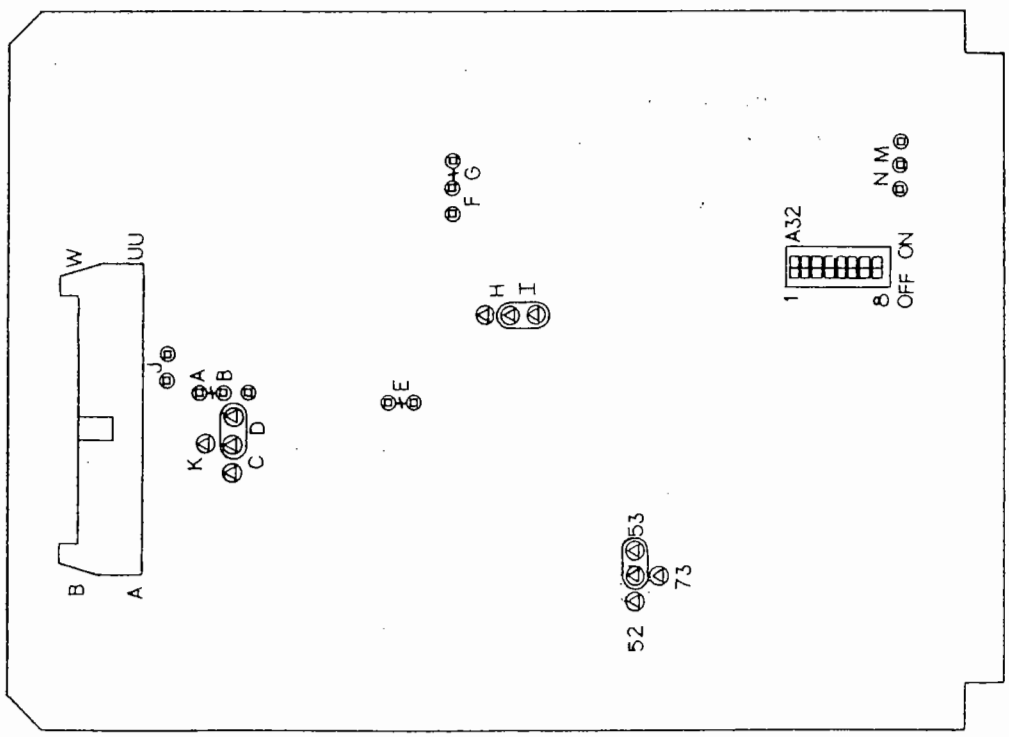


Figure B.12 Model 3553 Graphics Plotter Interface

DIP Switch (A32, lower right section of the board) set to:

Switch	Position	Comment
1-4	See note	
5	OFF	8 characters
6	ON	Disable Parity
7	ANY	Not Applicable
8	OFF	Two Stop Bits

Note: switches 1 through 4 set the Interface's Baud rate, which must correspond to the Printer/ Plotter's Baud rate. Refer to the Printer/ Plotter's instruction manual.

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see figure B.1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer (see figure B.1).
8. Locate the socket number marked on the chip (see figure B.9 for location).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.12 MODEL 3553 GRAPHICS PLOTTER INTERFACE

Models 3551, 3552A, and 3553 are mutually exclusive. Only one of these may be installed in the Analyzer.

The Model 3553 Graphics Plotter Interface consists of; a printed circuit board with an attached cable terminated in a 25-pin connector; an identifying decal; an interconnecting cable; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly. See figure B.12.

52/53/73 jumper in the 53 position
C-D jumper in the D position
H-I jumper in the I position
M-N jumper in the N position for line plot
M-N jumper in the M position for point plot

DIP Switch (A32, lower right section of the board) set to:

Switch	Position	Comment
1	ON	
2	OFF	Switches 1-4 set for
3	ON	2400 Baud
4	OFF	
5	OFF	8 characters
6	ON	Disable Parity
7	ANY	Not Applicable
8	OFF	Two Stop Bits

To Install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see figure B.1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer (see figure B.1).
8. Locate the socket number marked on the chip (see figure B.9 for location).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.13 MODEL 3554 MAGNETIC TAPE INTERFACE

The Model 3554 Mag Tape Interface consists of: a printed circuit board, a cable terminated in a 25-pin connector and a flat plastic connector; an identifying decal, an interconnecting cable; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers are set correctly. Refer to figure B.13.

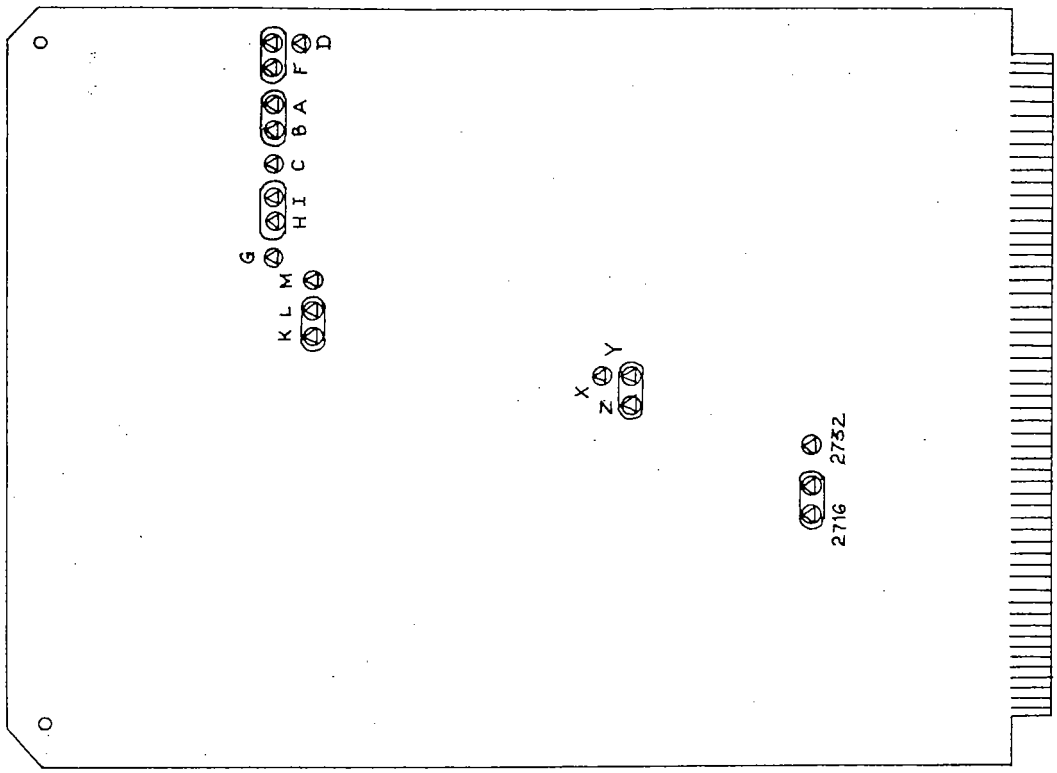


Figure B.13 Model 3554 Mag Tape Interface

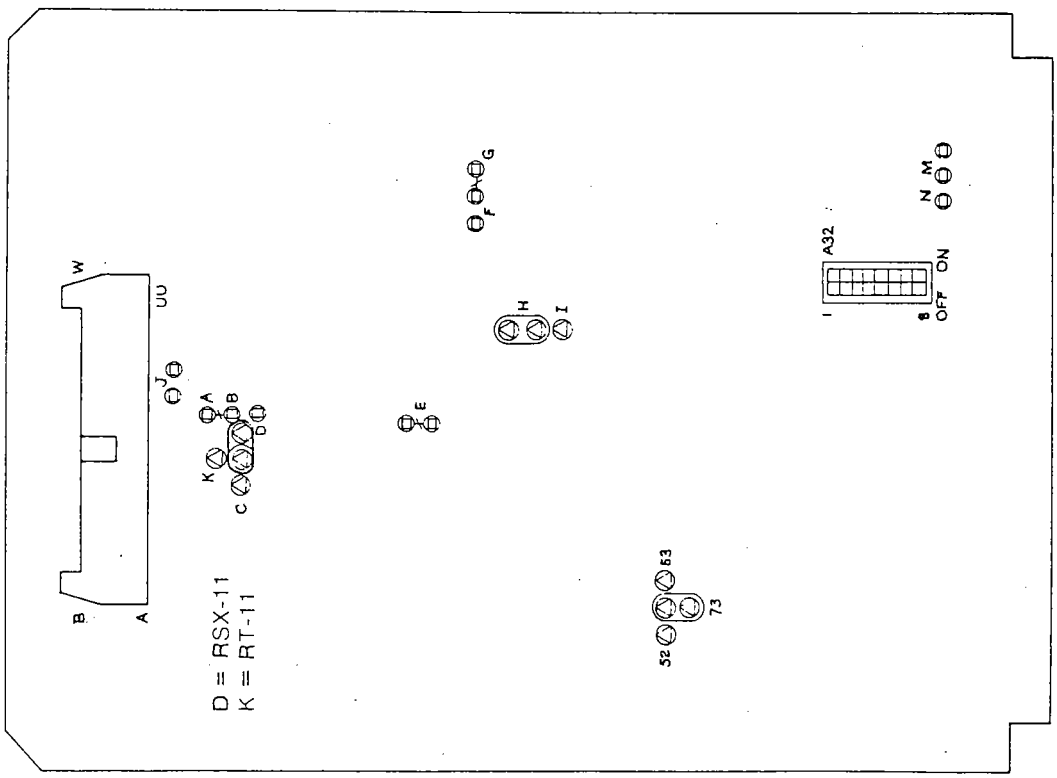


Figure B.14 Model 3571 Computer Interface

The factory settings are: A-B, E-F, H-I, K-L, Y-Z, 2716. Appendix A.9 details the use of other jumper positions.

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in the rear I/O slot in the Analyzer's Mother Board (see figure B.1). If there already is a board in this slot, pull it out and move it to the front I/O slot.
3. Plug the board's cable into the socket at the top of the board and install the 25-pin connector in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer.
8. Locate the socket number marked on the chip (see figure B.9 for location).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

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10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.14 MODEL 3571 COMPUTER INTERFACE

The Model 3571, 3572, 3573, and 3573B are mutually exclusive. Only one of these can be installed in the Analyzer.

The Model 3571 Computer Interface includes: a printed circuit board with an attached cable which is terminated in a 25-pin connector; two programmed integrated circuit chips marked with the Model number, the Firmware version number and a socket number; and an identifying decal.

The Firmware version number on the chips must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly. (See figure B.14):

52/53/73 jumper in the 73 position.
C-D jumper in the D position for RSX-11 systems, or in the K position for RT-11 systems.
H-I jumper in the H position.
M-N jumper out (not used with Model 3571).

DIP switch (A32) set to:

Switch	Position	Comment
1	ON	
2	OFF	Switches 1 - 4 Set
3	OFF	for 9600 Baud
4	OFF	
5	OFF	8 Characters
6	OFF	Enables Parity
7	OFF	Even Parity
8	ON	One Stop Bit

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see figure B.1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer (see figure B.1).
8. Locate the socket number marked on each chip (see figure B.9 for location).
9. Install the chips in the correct CPU Board locations.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that each chip is plugged in with the notch in the chip toward the right side of the board; the socket has a notch at the top as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

---

10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the Analyzer's covers, check the installation for proper operation.

B.15 MODEL 3572 GPIB

The Models 3571, 3572, 3573, and 3573B are mutually exclusive. Only one of these may be installed in the Analyzer.

The Model 3572 GPIB Interface consists of the Interface Board, an identifying decal, a programmed integrated circuit (chip), and a ribbon cable. One end of the cable plugs into the board; the other end mounts on the Analyzer's rear panel.

Before installing the Interface, be sure that the B0/B8 jumper is in the B0 position (figure B.15).

The eight switches in S1 must be set before installing the board (see figure B.15). Refer to Appendix B of the Model 3572 manual for a description of the switch functions.

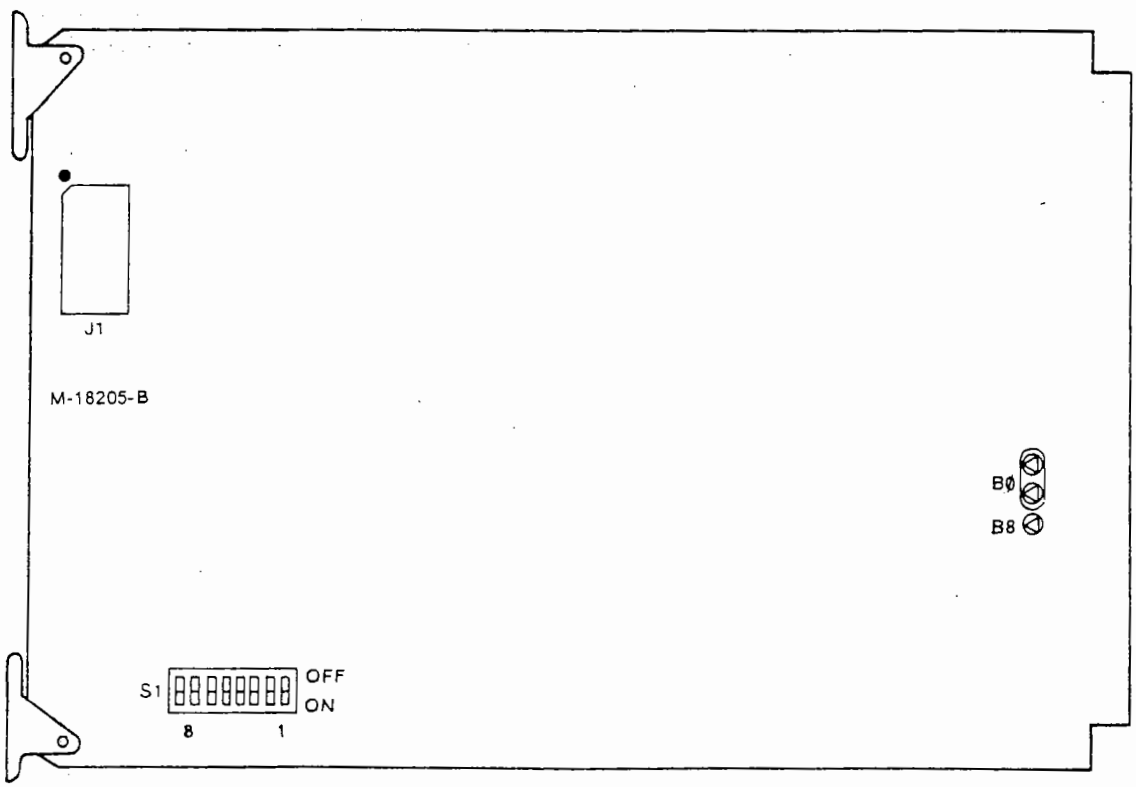

Figure B.15 Model 3572 GPIB Interface

To install the option:

1. Remove the CPU Board and locate the socket number marked on the chip (see figure B.9).
2. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a corresponding notch as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

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3. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
4. Install the Interface Board in one of the Option Board slots (see figure B.1).
5. Remove the cover plate from J107 on the rear panel.
6. The standoffs are not needed; they may be discarded.
7. Remove the nuts from the two supplied jackscrews and mount the ribbon-cable connector on the J107 opening.
8. Pass the jackscrews through the mounting holes on the connector and through the opening's screw holes.
9. Place the two lockwashers on the jackscrews inside the rear panel.
10. Put the nuts on the jackscrews and tighten them down securely.
11. Fold about 5 cm (2 in.) of the ribbon cable down on the right side of the Interface Board. This will prevent the connector from pulling out of the board's socket.

12. Pass the rest of the cable to the left across the top of the other boards. Place any slack in the cable inside the Monitor Compartment.
13. Place the supplied identifying decal on the rear panel connector.
14. Before replacing the covers, check the installation for proper operation.

B.16 MODELS 3573 and 3573B COMPUTER INTERFACES

The Models 3571, 3572, 3573, and 3573B are mutually exclusive. Only one of these may be installed in the Analyzer.

The Model 3573 and 3573B Computer Interfaces consist of: a printed circuit board with an attached cable, which is terminated in a 35-pin connector; two programmed integrated circuits (chips) marked with the Model number, the Firmware version number and a socket number; and an identifying decal.

Refer to the Model 3573 Operator's Manual for complete details on the two Interfaces.

The Firmware version number on the chip must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see figure B.2).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly.

M-N jumper out (not used with Model 3573).
52/53/73 jumper in the 73 position
To configure the Interface Board to your specific application, refer to the Model 3573 Operator's Manual for the switch settings and positioning of the other jumpers.

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See figure B.4.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see figure B.1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer.
8. Locate the socket number marked on the chip (see figure B.9 for location).
9. Install the chips in the correct CPU Board locations.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket.

Be sure that the chip is plugged in with the notch in the chip toward the right side of the board; the socket has a notch at the top as a guide.

CAUTION

Inserting a chip reversed will cause permanent damage to the chip when power is applied.

Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

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10. Move the CPU Board's D-E jumper to the E position for about one minute, then move it back to D. Replace the board in the Analyzer.
11. Before replacing the Analyzer's covers, check the installation for proper operation.

APPENDIX C
ADC ZERO ADJUSTMENT METHODS

This appendix describes two ways that the ADC's Zero can be adjusted for the ADC Gain being used: The Energy Calibrate Method and the Precision Pulser Method. The Pulser method is the most exact, but the Energy Calibrate method is acceptable under most circumstances. When the ADC is properly zeroed, the Calibration Equation's last term will be about equal to zero. The ZERO should be readjusted each time the ADC GAIN is changed, but it is not critical.

C.1 ENERGY CALIBRATE METHOD

A basic method of adjusting the ZERO is outlined in the following steps:

1. Collect a spectrum and Energy Calibrate it (see section 4.13).
2. Make a note of the displayed energy equation.
3. Divide the equation's offset term by the energy per channel.
4. The result is the number of channels that the spectrum must be moved with the ZERO control so that zero energy falls in channel zero.
5. Clear the memory, disable ECAL, and adjust the ZERO so that the spectrum's peaks move that number of channels from their previous location. Repeatedly clearing the memory will aid in the correct placement of the peaks.
6. If the offset term displayed was a negative number, the spectrum must be moved leftward.
7. If the offset term displayed was a positive number, the spectrum must be moved right.

C.2 PULSER METHOD

The most accurate method uses Canberra's Model 8210 Precision Pulser, or equivalent.

1. Set the Series 35 PLUS's MEMORY switch to:
   1/2 for the Model 3501 (displays 1024 channels)
   1/4 for the Model 3502 (displays 1024 channels)
   1/4 for the Model 3503 (displays 2048 channels)

2. Connect the Pulser to the ADC IN Connector with the ADC IN switch in the EXT position.
3. Set the Pulser's controls to HI, 0°, + and 0.5 µsec Rise Time.
4. Set the ADC GAIN and OFFSET as necessary for whichever baseline is to be determined:

GAIN	TOTAL OFFSET	OFFSET SWITCHES UP
8192	7168	1024, 2048, 4096
4096	3072	1024, 2048
2048	1024	1024
1024	none	none

NOTE: ADC Gains of 256 and 512 use the same ZERO setting as the 1024 Gain.

5. Set all of the binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY switch ON and adjust the COARSE and FINE AMPLITUDE controls so that the analyzer is collecting in channel 1023. It will be helpful to enable WINDOW to verify single channel collection.
6. Set the Series 35 PLUS's OFFSET to zero (all switches down) and set the upper six binary switches on the Model 8210 to OFF (the left-hand position).
7. Adjust the ZERO control on the Series 35 PLUS so that the analyzer is collecting in the proper channel as follows:

GAIN	CHANNEL
8192	127
4096	63
2048	31
1024	15

8. Repeat steps 4 through 7 until no further adjustments are necessary. In most cases, one repetition will be sufficient.
9. Note that the ZERO adjustment is made only for the one ADC GAIN setting being used. The ZERO need not be adjusted again unless another ADC GAIN is selected for use.

APPENDIX D
COMPUTATIONAL METHODS

D.1 INTEGRAL

The Integral is the total number of counts in the region. The region is defined to extend from the left current ROI channel to the right current ROI channel, inclusive.

If no ROI exists, the Integral is calculated for the entire displayed memory.

$$\text{INTEGRAL} = \sum_{a=u}^{v} X_a$$

D.2 PEAK AREA

The Area algorithm computes the number of counts in a region above the background. The region is defined as the peak plus the specified end-points. The background is determined by averaging K points on either side of the peak, then drawing a straight line between the two averaged values.

$$\text{AREA} = \text{INTEGRAL} - \text{BACKGROUND AREA}$$
$$\text{BACKGROUND AREA} = [(N/2)\cdot(B_1+B_2)]$$

where

$N = v-u+1$; the number of data channels in the ROI
u = the ROI's start channel
v = the ROI's stop channel

$B_1 = \left(\sum_{a=u}^{u+K-1} X_a\right) \div K$; averaged height of the background on the left

$B_2 = \left(\sum_{a=v-K+1}^{v} X_a\right) \div K$; averaged height of the background on the right

$K = 4$, the number of end-points considered
X_u = counts in channel u
X_v = counts in channel v

This is shown graphically in Figure D.1.

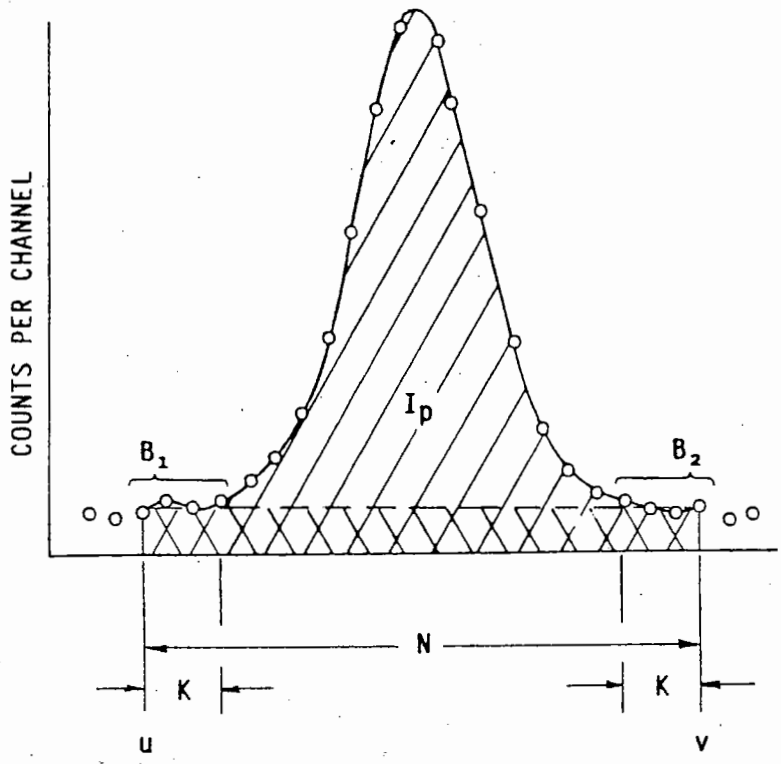


Figure D.1 Typical Spectrum Peak

D.3 STRIP

Y' = Y-F x X, where X and Y are two spectra in memory. The strip factor, F, may be any operator-specified value in the range:

$$-327.675 < F < +327.675$$

The resultant spectrum (Y') replaces spectrum Y (the original spectrum); spectrum X is unchanged.

D.4 FWHM

The Full Width Half Maximum (FWHM) algorithm calculates the current peak's width at half of its maximum amplitude. The calculation proceeds as follows:

a) The current ROI determines the search limits and the background.

b) The highest channel within this ROI, corrected for the background, is located using 3-point smoothed data.

c) Half Maximum value equals the counts in the highest channel (determined by a 3-point smooth) background corrected and divided by 2. If a divide error occurs, the algorithm will report zero.

d) Using data in the highest channel, proceed down each side to locate the channel whose counts fall below the designated Half Maximum value. The left and right FWHM points are the interpolated channels between the counts of the channel below the Half Maximum value and the counts of the channel above the Half Maximum value.

e) Full Width Half Maximum is the delta between the interpolated half maximum channels.

NOTE: Results may be misleading and insignificant if data is smoothed on narrow peaks to determine both the highest channel and Half Maximum values. Therefore, raw (unsmoothed) data is used for peaks of 20 channels or less.

D.5 CENTROID

The Centroid is the geometric "center of gravity" of the peak; it is not usually located at an exact channel number.

a) Proceeding from the left Half Maximum point (channel below the Half Maximum value) to the right Half Maximum point, compute:

$$I_C = \frac{\Sigma(I \cdot C_I)}{\Sigma\ C_I}$$

where C_I = absolute contents of Channel I
I = channel address relative to the left Half-Maximum point.

b) Peak Centroid then equals left Half-Maximum point + I_C.

D.6 AUTOMATIC PEAK SEARCH

The peak search mode locates all valid peaks in a Germanium detector spectrum, as defined by the factors set in the Menu. The various formulae used in determining a valid peak are as follows:

where X_i = counts in the i^{th} channel.
sigma = square root of Xi ($\sqrt{Xi}$).
C_L = left search limit
C_R = right search limit.

a) PEAK START: Using raw channel data; the peak start channel is that channel at which:

1) $i < C_R$ AND
2) $Xi_{+1} - \text{sigma} > Xi > Xi_{-1} + \text{sigma}$

b) Peak Top: The peak channel is the first channel after X_i before a decrease in height or leveling, using 3-point smoothed data and $i<C_R$

c) Peak Stop: Using raw channel data and starting at the first channel after the peak top channel plus 1, the peak start channel is that channel at which:

1) $i \leq C_R$ AND
2) $Xi \leq Xi_{+1}$

If all of the above conditions are met, then the validity of the peak is checked using the following criteria:

1) $P_{stop} - P_{start} \geq P_{min}$

2) $X_m - X_{start}) \geq \text{sigma} \cdot \sqrt{X_{start} + X_m}$

where P_{stop} = peak stop channel
P_{start} = peak start channel
X_m = counts at the top of the peak
X_{start} = counts at the peak start channel
Sigma: if $X_{start} < 200$, then
Sigma = 15 • (Peak Sigma $\div\sqrt{X_{start}+25}$)
if $X_{start} \geq 200$, then
Sigma = Peak Sigma (where peak sigma was determined in "analyz factor").

D.7 SMOOTH

Smooth averages data between the left and right cursors, inclusive.

$$Y_i = \frac{Y_{i-1} + 2Y_i + Y_{i+1}}{4}$$

where Y_i = the contents of channel i.

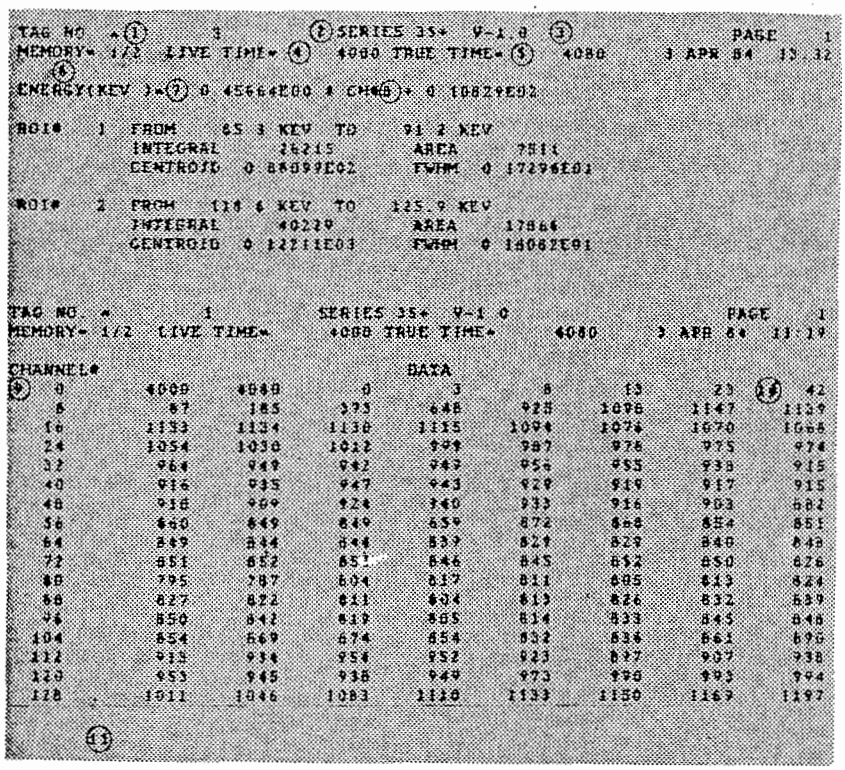
APPENDIX E
INPUT/OUTPUT FORMATS

E.1 ASCII I/O MODE

ITEM	IDENTIFIER CODE (octal)	FIELD
1 TAGWORD	5	8 ASCII digits, leading spaces
2 HEADER ID	2	24 ASCII characters
3 TERMINATE Header and variable length fields	3	
4 LIVE TIME or SWEEPS	36	8 ASCII digits, leading spaces
5 TRUE TIME or DWELL TIME	37	8 ASCII digits, leading spaces
6 UNITS	11	EV, KEV, MEV, MSEC, SEC, MIN
7 "B" coefficient	7	Floating Point FIELD, variable length terminated by Octal 3
8 "C" coefficient	10	Floating Point FIELD, variable length terminated by Octal 3
9 ASCII Address	33	5 digits, leading spaces
10 ASCII DATA	17	8 digits, leading spaces
11 END OF DATA	4	(EOT) Always used to terminate tape transmission

In ASCII mode, bit 8 is parity for each character (byte).
Each line ends with: CR NU NU NU NU LF

Each of the items described in this list is shown in figure E.1.



```
TAG NO. =(1)      3          (2)SERIES 35+  V-1.0  (3)                PAGE    1
MEMORY= 1/2  LIVE TIME= (4)   4080 TRUE TIME= (5)   4080     3 APR 84  13:12
 (6)
ENERGY(KEV )=(7) 0 45664E00 # CH=(8)= 0 10829E02

ROI#   1  FROM    65.3 KEV  TO    91.2 KEV
          INTEGRAL     16215        AREA      7511
          CENTROID  0 88099E02      FWHM  0 17296E01

ROI#   2  FROM   114.6 KEV  TO   125.9 KEV
          INTEGRAL     40229        AREA     17866
          CENTROID  0 12711E03      FWHM  0 14062E01


TAG NO. =       1          SERIES 35+  V-1.0                    PAGE    1
MEMORY= 1/2  LIVE TIME=     4080 TRUE TIME=      4080     3 APR 84  13:19

CHANNEL#                          DATA
(9)   0      4089     4048       0        3        8       13       23  (10) 42
      6        87      185      373      648      928     1098     1147     1139
     12      1133     1134     1130     1115     1094     1074     1070     1066
     18      1054     1030     1012      991      987      978      975      974
     24       964      949      942      943      956      955      938      915
     30       916      935      947      943      929      919      917      915
     36       918      909      924      940      933      916      903      882
     42       860      849      849      859      872      888      884      851
     48       849      844      844      839      821      829      840      848
     54       851      852      851      846      845      852      850      826
     60       795      787      804      817      811      805      813      824
     66       827      822      811      804      813      826      832      839
     72       850      842      819      805      814      833      845      848
     78       854      869      874      854      832      836      861      870
     84       913      914      954      952      923      897      907      938
     90       953      945      938      949      973      990      993      994
     96      1011     1046     1083     1110     1133     1150     1169     1197
(11)
```

Figure E.1
ASCII Readout
Example

E.2 SERIES 35 PLUS BINARY MODE OF I/O

The memory data is transferred in a binary format. Each Region to be transferred is organized into a Data Block with the following characteristic:

Identifier Code $(34)_8$

Region Channel Count Low Byte		
Region Channel Count High Byte		(n)
Starting Channel Address Low Byte		
Starting Channel Address High Byte		
Data High Byte	Data from first	(1)
Data Low Byte	Channel in region	|
Data Middle Byte	|	|
	|	|
	|	|
Data High Byte	Data from last	|
Data Low Byte	channel in region	(n)
Data Middle Byte		

The tape output will be:

- Title and Header as in ASCII mode
- Data Block 1
- Data Block m
- EOT $(4)_8$

Parity: In Binary mode, no parity is maintained.

APPENDIX F
STANDARD AP-PAK EQUATIONS

NOTE: In all equations, ROI #0 means the current ROI; that is, the ROI where the cursor is currently located or the next ROI to the cursor's right if it is not in an ROI.

Equation Number	Name	Definition
5	Minimum Detectable Activity	(3•SQRT(V2-V1))÷(TL•K1•K2•3.7E4), where K1 = Gammas per disintegration, K2 = Results of Equ #11, V1 = AREA of ROI #0, and V2 = INT of ROI #0.
6	Compton Edge	V1÷(1+(255.5÷V1)), where V1 = Centroid (in keV) of ROI #0.
7	Counts/ Second	V1/TL, where V1 = AREA of ROI #0.
8	Percent Error	165•((SQRT(V1))/V1), where 165 = 90% confidence x 100%, and V1 = AREA of ROI #0.
9	Percent Dead Time	((V1-TL)V1)•100 where V1 = CNT at CH#1.
10	Half Life	K1, where K1 = the isotope's half life

11	Efficiency	(V1/TL)/(K1•EXP(-0.693•K2/V2)), where K1 = Gammas/sec, K2 = Decay time in the same time units as Equation #10, V1 = AREA of ROI #0, and V2 = Equation #10.
12	Activity in µCi	(V1/TL)/(3.7E4•K1•K2) where K1 = Gammas/disintegration, K2 = The results of Equation #11. V1 = AREA of ROI #0, and
13	Decay Corrected Activity	V1/EXP(-0.693•K1/V2), where K1 = Decay time in the same time units as Equation #10, V1 = Equation #12, and V2 = Equation #10.
14	Dose Rate mR/hr	(0.53•K1•V1•1E-6)/(K2•K2), where K1 = Yield (Gammas per disintegration) K2 = Detector-to-source distance in meters, V1 = Equation #12.

APPENDIX G
MODEL 3543 ISOTOPE LIBRARY

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
1	NA-22	2.60 Y	511.0	0.0
			1274.5	99.9
2	NA-24	15.00 H	1368.5	100.0
			2754.1	99.9
3	K-40	1.28E09 Y	1460.8	10.7
4	CR-51	27.70 D	320.1	9.8
5	MN-54	312.50 D	834.8	100.0
6	CO-56	77.30 D	511.0	0.0
			846.8	100.0
			1037.8	14.0
			1238.2	67.6
			1771.5	15.7
			2598.6	16.9
			3253.6	7.4
7	MN-56	2.58 H	846.8	98.9
			1810.7	27.2
			2113.1	14.3
8	CO-57	270.89 D	122.1	85.6
			136.5	10.6
9	CO-58	70.80 D	511.0	0.0
			810.8	99.5
10	FE-59	44.60 D	1099.2	56.5
			1291.6	43.2
11	CO-60	5.27 Y	1173.2	99.9
			1332.5	100.0
12	ZN-65	244.09 D	1115.5	50.8
13	KR-85M	4.50 H	151.2	75.5
			304.5	14.0
14	SR-85	64.70 D	514.0	99.3

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
15	KR-87	1.27 H	402.6	49.5
16	KR-88	2.84 H	196.3	26.3
			834.8	13.1
			1529.8	11.1
			2195.8	13.3
			2392.1	35.0
17	Y-88	106.60 D	898.0	94.0
			1836.0	99.4
18	KR-89	3.17 M	220.9	20.4
			585.8	16.9
19	RB-89	15.20 M	657.7	10.1
			947.7	9.4
			1031.9	59.0
			1248.1	43.0
			2196.0	13.6
			2570.1	10.0
20	SR-91	9.50 H	652.7	11.1
			749.8	23.1
			1024.3	33.5
21	Y-91M	49.70 H	557.6	95.1
22	NB-95	35.20 D	765.8	100.0
23	ZR-95	64.00 D	724.2	44.5
			756.7	55.0
24	RU-103	39.40 D	497.1	86.4
25	CD-109	453.00 D	88.0	3.8
26	AG-110M	252.20 D	657.7	94.7
			706.7	16.4
			884.7	73.0
			937.4	34.4
			1384.3	24.7
			1505.0	13.3
27	SN-113	115.00 D	391.7	64.2

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
28	SB-124	60.20 D	602.7	97.9
			722.8	11.3
			1691.0	48.8
29	SB-126	12.40 D	414.8	85.7
			666.2	99.6
			695.0	99.6
			697.0	31.9
			720.5	57.8
			856.7	17.0
30	I-131	8.04 D	80.2	2.6
			284.3	6.1
			364.5	81.2
			637.0	7.3
			722.9	1.8
31	XE-131M	11.90 D	163.9	2.0
32	I-132	2.30 H	505.9	5.0
			522.7	16.1
			630.2	13.7
			667.7	98.7
			772.6	76.2
			954.6	18.1
33	BA-133	10.70 Y	80.9	35.2
			276.4	7.3
			302.8	18.6
			356.0	62.3
			383.8	8.8
34	I-133	20.80 H	529.9	87.3
			875.4	4.4
35	XE-133	5.25 D	81.0	37.0
36	XE-133M	2.19 D	233.2	10.3
37	CS-134	2.06 Y	563.2	8.4
			569.3	15.4
			604.7	97.6
			795.8	85.4
			801.9	8.7

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
38	I-134	52.60 M	405.5	7.3
			540.8	7.8
			595.4	11.4
			621.8	10.6
			677.3	8.5
			847.0	95.4
			857.3	7.0
			884.1	65.3
			1072.6	15.3
			1136.2	9.7
			1806.8	5.7
39	I-135	6.61 H	546.6	7.1
			1038.8	7.9
			1131.5	22.5
			1260.4	28.6
			1457.6	8.6
			1678.0	9.5
			1706.5	4.1
			1791.2	7.7
40	XE-135	9.08 H	249.8	89.9
			608.2	2.9
41	XE-135M	15.70 M	526.6	81.0
42	CS-136	13.10 D	153.2	7.5
			176.6	13.6
			273.7	12.7
			340.6	46.8
			818.4	99.7
			1048.1	79.8
			1235.3	19.7
43	CS-137	30.20 Y	661.6	85.1
44	CS-138	32.20 M	462.8	30.7
			546.9	10.8
			1009.8	29.8
			1435.9	76.3
			2218.0	15.2
			2639.6	7.6

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
45	XE-138	14.20 M	153.8	6.0
			258.3	31.9
			396.4	6.3
			434.5	20.3
			1768.3	16.7
			2015.8	12.3
46	BA-139	82.70 M	165.9	18.8
47	CE-139	137.50 D	165.9	80.0
48	BA-140	12.80 D	537.3	20.0
49	LA-140	40.20 H	328.8	18.5
			487.0	43.0
			815.9	22.5
			1596.5	95.6
50	CE-141	32.50 D	145.4	48.0
51	CE-144	284.30 D	133.5	10.8
52	TA-182	115.00 D	58.0	8.5
			67.7	46.5
			100.0	14.1
			152.4	7.2
			222.1	7.6
			1121.3	35.0
			1189.0	16.5
			1221.4	27.4
			1231.0	11.6
53	W-187	23.90 H	72.1	11.9
			134.2	9.4
			479.5	23.4
			551.6	5.5
			618.4	6.7
			685.8	29.2
			772.9	4.4
54	HG-203	46.60 D	72.9	6.4
			279.0	81.5

	ELEMENT NAME	HALF LIFE	ENERGY (keV)	YIELD (%)
55	BI-207	38.00 Y	72.8	23.0
			75.0	38.6
			84.8	14.0
			569.7	98.0
			1063.6	77.0
			1770.2	7.0
56	BI-214	19.90 M	609.3	46.1
			1120.3	15.0
			1764.5	15.9
57	PB-214	26.80 M	241.9	7.5
			295.2	19.2
			351.9	37.0
58	U-235	7.0999E08 Y	143.8	10.5
			185.7	54.0
59	NP-237	2.1001E06 Y	29.4	9.8
			86.5	13.1
60	NP-239	56.50 H	106.1	22.7
			228.2	10.7
			277.6	14.1
			315.9	1.6
			334.2	2.0
61	PU-239	2.4399E04 Y	52.0	0.0
			129.0	0.0
			375.0	0.0
62	AM-241	432.99 Y	59.5	36.3

PRIMARY REFERENCE:

Nuclear Decay Data for Radionuclides Occurring in Routine Releases from Nuclear Fuel Cycle Facilities, D. C. Kocher, ORNL/NUREG/TM-102, 1977.

SECONDARY REFERENCE:

The Gamma Rays of the Radionuclides, Vol. 7, G. Erdtmann and W. Soyka, 1979, Verlag Chemie.

Radionuclides referenced within this Library may change without notice.

APPENDIX H
MODEL 3544 X-RAY LIBRARY

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
NA 11	KA12	100	1.041						
MG 12	KA12	100	1.253						
AL 13	KA12	150	1.486						
SI 14	KA12	150	1.739						
P 15	KA12	150	2.013						
S 16	KA12	150	2.307						
CL 17	KA12	150	2.621						
	KB	8	2.815						
AR 18	KA12	150	2.957						
	KB13	15	3.190						
K 19	KA12	150	3.312						
	KB13	15	3.589						
CA 20	KA12	150	3.690						
	KB13	15	4.012						
SC 21	KA12	150	4.088						
	KB13	20	4.460						
TI 22	KA12	150	4.508						
	KB13	20	4.931						

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
V 23	KA12	150	4.949						
	KB13	20	5.426						
CR 24	KA12	150	5.411						
	KB13	18	5.946						
MN 25	KA12	150	5.894						
	KB13	20	6.489						
FE 26	KA12	150	6.398						
	KB13	20	7.057						
CO 27	KA12	150	6.924						
	KB13	20	7.648						
NI 28	KA12	150	7.471						
	KB13	20	8.263						
CU 29	KA12	150	8.040						
	KB13	20	8.904						
ZN 30	KA12	150	8.630						
	KB13	20	9.570						
GA 31	KA12	150	9.241						
	KB13	21	10.262						
GE 32	KA12	150	9.874						
	KB13	21	10.979						
AS 33	KA12	150	10.530						
	KB13	22	11.722						
SE 34	KA12	150	11.207						
	KB13	24	12.492						

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
BR 35	KA12	150	11.907						
	KB13	24	13.287						
KR 36	KA12	150	12.631						
	KB13	24	14.107						
RB 37	KA12	150	13.373						
	KB13	24	14.956						
SR 38	KA12	150	14.140						
	KB13	24	15.829						
Y 39	KA12	150	14.931						
	KB13	24	16.731						
ZR 40	KA12	150	15.744	LA12	110	2.042			
	KB13	24	17.660	LB1	45	2.124			
NB 41	KA12	150	16.581	LA12	110	2.166			
	KB13	8	18.604	LB1	45	2.257			
	KB	4	18.949						
MO 42	KA12	150	17.441	LA12	110	2.293			
	KB13	24	19.600	LB1	45	2.394			
TC 43	KA12	150	18.325	LA1	100	2.424			
	KB13	24	20.608	LB1	45	2.536			
RU 44	KA12	150	19.233	LA12	110	2.558			
	KB13	24	21.646	LB1	55	2.698			
RH 45	KA12	150	20.165	LA12	110	2.696			
	KB13	24	22.712	LB1	86	2.899			

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
PD 46	KA12	150	21.121	LA12	110	2.838			
	KB13	26	23.806	LB12	84	3.059			
AG 47	KA12	150	22.101	LA12	110	2.983			
	KB13	26	24.928	LB12	84	3.224			
CD 48	KA12	150	23.106	LA12	110	3.132			
	KB13	27	26.081	LB1	59	3.337			
				LB2	25	3.528			
IN 49	KA2	50	23.998	LA12	110	3.285			
	KA1	100	24.206	LB1	86	3.496			
	KB13	27	27.260	LB2	17	3.713			
SN 50	KA2	50	25.040	LA12	110	3.442			
	KA1	100	25.267	LB1	86	3.671			
	KB13	28	28.467	LB2	17	3.904			
SB 51	KA2	50	26.106	LA12	110	3.603			
	KA1	100	26.355	LB1	86	3.853			
	KB13	29	29.706	LB2	17	4.100			
TE 52	KA2	50	27.197	LA12	110	3.768			
	KA1	100	27.468	LB1	86	4.039			
	KB13	29	30.974	LB2	17	4.301			
I 53	KA2	50	28.312	LA12	110	3.936			
	KA1	100	28.607	LB1	86	4.230			
	KB13	29	32.272	LB2	17	4.507			
XE 54	KA2	50	29.453	LA1	100	4.109			
	KA1	100	29.774						
	KB13	29	33.599						
CS 55	KA2	50	30.620	LA12	110	4.285			
	KA1	100	30.968	LB1	61	4.631			
	KB13	30	34.961	LB2	20	4.935			

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
BA 56	KA2	50	31.812	LA12	110	4.464			
	KA1	100	32.188	LB1	61	4.839			
	KB13	28	36.353	LB2	20	5.156			
LA 57	KA2	50	33.028	LA12	110	4.648			
	KA1	100	33.436	LB1	61	5.053			
	KB13	30	37.771	LB2	20	5.383			
CE 58	KA2	50	34.273	LA12	110	4.837			
	KA1	100	34.714	LB1	61	5.272			
	KB13	32	39.233	LB2	20	5.612			
PR 59	KA2	50	35.544	LA12	110	5.031			
	KA1	100	36.020	LB1	61	5.499			
	KB13	32	40.711	LB2	20	5.849			
	KB2	65	41.767						
ND 60	KA2	50	36.841	LA12	110	5.227			
	KA1	100	37.355	LB1	61	5.732			
	KB13	32	42.231	LB2	20	6.088			
PM 61	KA2	50	38.165	LA12	110	5.430			
	KA1	100	38.718	LB1	56	5.972			
	KB13	32	43.783	LB2	20	6.338			
SM 62	KA2	50	39.516	LA12	110	5.632			
	KA1	100	40.111	LB1	61	6.214			
	KB13	32	45.366	LB2	20	6.586			
EU 63	KA2	50	40.895	LA12	110	5.842			
	KA1	100	41.535	LB1	61	6.465			
	KB13	34	46.987	LB2	20	6.842			
GD 64	KA2	50	42.302	LA12	110	6.053			
	KA1	100	42.989	LB1	61	6.721			
	KB13	34	48.642	LB2	20	7.102			

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
TB 65	KA2	50	43.737	LA12	110	6.269			
	KA1	100	44.474	LB1	61	6.985			
	KB13	34	50.325	LB2	20	7.365			
DY 66	KA2	50	45.200	LA12	110	6.491			
	KA1	100	45.991	LB1	61	7.215			
	KB13	34	52.051	LB2	20	7.634			
HO 67	KA2	50	46.692	LA12	110	6.715			
	KA1	100	47.539	LB1	61	7.532			
	KB13	33	53.813	LB2	20	7.910			
ER 68	KA2	50	48.213	LA12	110	6.943			
	KA1	100	49.119	LB1	61	7.816			
	KB13	34	55.606	LB2	20	8.188			
TM 69	KA2	50	49.764	LA12	110	7.175			
	KA1	100	50.733	LB1	61	8.106			
	KB3	11	57.293	LB2	20	8.467			
	KB1	23	57.506						
YB 70	KA2	50	51.345	LA12	110	7.410			
	KA1	100	52.380	LB1	61	8.406			
	KB3	12	59.141	LB2	20	8.757			
	KB1	64	59.356						
LU 71	KA2	50	52.956	LA12	110	7.649			
	KA1	100	54.061	LB1	61	8.713			
	KB3	12	61.037	LB2	20	9.038			
	KB1	65	61.272						
HF 72	KA2	50	54.602	LA12	110	7.893			
	KA1	100	55.781	LB1	60	8.919			
	KB3	12	62.969	LB2	20	9.346			
	KB1	66	63.222						
TA 73	KA2	50	56.267	LA12	110	8.140			
	KA1	100	57.523	LB1	60	9.348			
	KB3	12	64.938	LB2	20	9.650			
	KB1	26	65.212						

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
W 74	KA2	50	57.972	LA12	110	8.390			
	KA1	100	59.308	LB1	54	9.660			
				LB2	26	9.927			
RE 75	KA2	50	59.708	LA12	110	8.645			
	KA1	100	61.130	LB1	54	9.996			
				LB2	27	10.248			
OS 76	KA2	50	61.476	LA12	110	8.904	MB	45	1.978
	KA1	100	62.990	LB1	54	10.341			
				LB2	27	10.578			
IR 77	KA2	50	63.276	LA12	110	9.167	MA12	200	1.977
	KA1	100	64.885	LB1	50	10.706	MB	45	2.053
				LB2	27	10.907			
PT 78	KA2	50	65.112	LA12	110	9.434	MA12	200	2.048
				LB1	50	11.069	MB	50	2.127
				LB2	26	11.245			
AU 79				LA12	110	9.704	MA12	200	2.120
				LB1	50	11.440	MB	50	2.204
				LB2	27	11.588			
HG 80				LA12	110	9.979	MA	100	2.195
				LB12	77	11.862	MB	20	2.282
TL81				LA12	110	10.258	MA12	200	2.267
				LB12	77	12.241	MB	55	2.362
PB 82				LA12	110	10.541	MA12	200	2.342
				LB12	77	12.628	MB	60	2.442
BI 83				LA12	110	10.827	MA12	200	2.419
				LB12	70	13.009	MB	60	2.525

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
PO 84				LA12	110	11.119			
				LB12	70	13.414			
				LB3	7	13.656			
AT 85				LA12	110	11.414			
				LB1	50	13.874			
				LB3	10	14.065			
RN 86				LA12	110	11.713			
				LB1	50	14.313			
				LB3	10	14.509			
FR 87				LA12	110	12.017			
				LB2	20	14.448			
				LB1	50	14.768			
				LB3	10	14.973			
RA 88				LA12	110	12.325			
				LB2	25	14.810			
				LB1	51	15.236			
AC 89				LA12	110	12.636			
				LB1	50	15.710			
				LB3	10	15.929			
TH 90				LA12	110	12.952	MA	200	2.991
				LB2	25	15.623	MB	60	3.145
				LB1	51	16.199			
PA 91				LA12	110	13.273	MA	200	3.077
				LB2	24	16.035	MB	60	3.239
				LB1	50	16.699			
U 92				LA12	110	13.596	MA	200	3.164
				LB2	24	16.450	MB	60	3.336
				LB1	50	17.217			

Element Z	Line K	I %	Energy in keV	Line L	I %	Energy in keV	Line M	I %	Energy in keV
NP 93				LA12	110	13.925			
				LB2	20	16.837			
				LB1	50	17.747			
PU 94				LA2	10	14.082			
				LA1	100	14.276			
				LB2	20	17.252			
				LB1	50	18.291			
AM 95				LA2	10	14.409			
				LA1	100	14.615			
				LB2	20	17.573			
				LB1	50	18.849			
CM 96				LA2	10	14.740			
				LA1	100	14.953			
				LB2	20	18.096			
				LB1	50	19.399			
BK 97				LA2	10	15.080			
				LA1	100	15.304			
				LB2	20	18.529			
				LB1	50	19.961			
CF 98				LA2	10	15.418			
				LA1	100	15.652			
				LB2	20	18.983			
				LB1	50	20.557			

Reference: X-RAY EMISSION WAVELENGTHS AND KEV TABLES FOR NONDIFFRACTIVE ANALYSIS

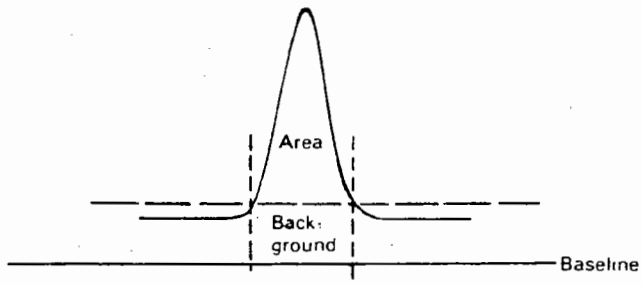
BY G. G. Johnson, Jr. and E. W. White
AMERICAN SOCIETY FOR TESTING AND MATERIALS
Data Series DS 46

GLOSSARY OF TERMS

ADC--Analog to Digital Converter. An electronic instrument which generates a digital word representing the magnitude of an analog signal.

ANTICOINCIDENCE GATING--The use of a logic pulse to trigger the rejection of a signal pulse by a signal processing device.

AREA--The number of counts in a given region that are above a determined background level. Equal to the region's integral minus the background.

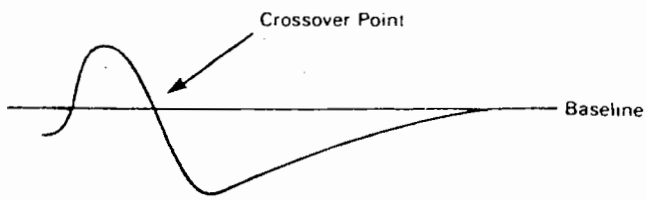


ASCII--American Standard Code for Information Interchange. A standard method of encoding alphabetical and numberical characters for digital transmission.

BASELINE--A reference from which a pulse excursion varies. Usually zero volts.

BASELINE, ADC--ZERO, ADC.

BIPOLAR PULSE--A pulse that has successive excursions in both the positive direction and the negative direction from the baseline.



BNC--A type of coaxial cable connector.

CHANNEL--An MCA memory location used to store one word of spectral data.

COINCIDENCE GATING--The use of a logic pulse to trigger the acceptance of a signal pulse by a signal processing device.

COLLECT--An MCA function that causes storage of data in memory.

COUNT RATE STABILITY--The degree to which the amplitude of a pulse is distorted by variations in the average pulse rate.

CONVERSION GAIN, ADC--The number of discrete voltage levels that the ADC's full scale input is divided into. Commonly a binary multiple of 256 channels.

CONVERSION TIME--The time required to change an input signal from one format to another, such as analog to digital; contributes to Dead Time.

CROSSOVER TIME--The time at which the bipolar pulse passes through a designated level; usually the baseline. See BIPOLAR illustration.

CRT--Cathode Ray Tube. A visual display device similar to a television receiver picture tube.

CURRENT LOOP--A continuous current path, usually carrying 20 milliamperes, between the sending unit and the printer.

CURSOR--A vertical marker in the MCA display. Can be moved to a channel or area of interest; the display shows cursor location and channel count as numeric data.

DEAD TIME--The time that the processing circuits are busy processing a signal and are not able to accept another pulse. Often expressed as a percentage.

DIFFERENTIAL NONLINEARITY--Maximum channel to channel deviation from the ideal uniformity of channel width. The measure of how nearly all channels have the same incremental voltage width.

DWELL TIME--The sampling interval per channel in the Multichannel Scaling mode of data acquisition.

EIA RS232C/RS422--(United States) Electronic Industries Association standards for transmitting digital information.

ENERGY CALIBRATION--An MCA function where the displayed energy spectrum is calibrated for a specific unit of energy per channel. Allows unknown energy peaks to be identified by their location in the calibrated spectrum.

FALL TIME CONSTANT--The time required for a pulse to fall from its original peak amplitude to 37% of its original peak amplitude.

FWHM--Full Width at Half Maximum. The full width of a distribution measured at half of the maximum amplitude. Defines spectrum resolution.

GAIN--The ratio of the amplifier's output signal to its input signal.

GPIB--General Purpose Interface Bus. Equivalent to the Hewlett-Packard Interface Bus (HPIB). Complies with IEEE-488 specifications.

GAUSSIAN PULSE SHAPE--A pulse shape resembling a statistical bell-curve and having little or no overshoot or ringing. See UNIPOLAR PULSE illustration.

HISTOGRAM--A representation of an energy peak by means of vertical bars, the heights of which indicate the frequency of the energy events.

IMPEDANCE MATCHING--The necessity of terminating a signal line in its characteristic impedance (listed in the product specifications) to allow optimum transfer of undistorted signals from one device to another.

INPUT/OUTPUT--The process of introducing data into or extracting data from an MCA using a peripheral recording device, such as a computer, a printer, a magnetic tape, or a cassette tape.

INDEX--An MCA function that jumps the cursor from one ROI to another.

INTEGRAL (MCA)--The sum of the absolute number of counts in all channels in a given region. See AREA illustration.

INTEGRAL NONLINEARITY--The measure of the deviation of a signal from a theoretical straight line between zero and its maximum value, expressed as a percentage of the full scale value.

INTENSIFY--A brighter region of the display which visually sets a Region of Interest off from data regions of lesser importance.

I/O--See INPUT/OUTPUT.

LINEARITY--Invariance (within specified limits) of amplitude and/or timing of an output with reference to the same input repeated over a significant period of time.

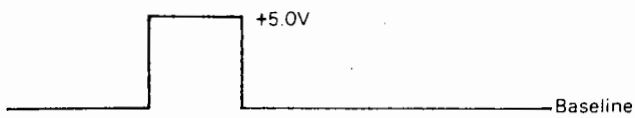
LIST--A data acquisition mode where each converted input is stored sequentially, one conversion per channel.

LIVE TIME--The time that the processing circuits are not busy processing a signal.

LIVE TIME CORRECTION--The process of stopping the Live Time clock in the MCA whenever the processing circuits are busy and can accept no further information. Commonly used to extend the collection time by accounting for the Dead Time.

LLD--Lower Level Discriminator--a comparator that outputs a logic pulse when the analog input exceeds a preset reference voltage level.

LOGIC PULSE--Generally refers to a TTL compatible logic pulse: 2.5 to 5.0 volts is a high level; less than 0.8 volts is a low level. Width is defined by use.



MCA--MultiChannel Analyzer.

MCS--MultiChannel Scaling. Distribution of events versus time.

MEMORY--An electronic device which acts as a data storage medium.

MIXER/ROUTER--An electronic instrument that accepts several inputs and routes each into a separate section of the MCA memory.

NIM--Nuclear Instrumentation Module.

NOISE--Unwanted disturbances on or with a useful signal which tend to obscure its information content.

NORMALIZE--An MCA function where data in a given area or in the whole memory is adjusted by addition of and/or multiplication by operator specified factors. Used to adjust the data so that it falls within a prescribed range.

OFFSET, ADC--A digitally performed shift in the zero channel of the ADC. Shifts the entire spectrum by the selected number of channels.

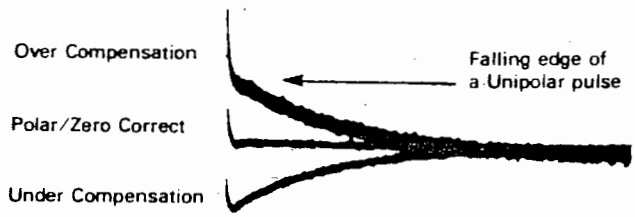
OVERLAP--An MCA function where a section of memory can be displayed with a reference section. Usually offset by some percentage of the reference section.

PEAK--A statistical distribution of digitized energy data for a single radioisotope.

PEAK CHANNEL--The channel number corresponding to the peak of a radioisotope's energy distribution.

PHA--Pulse Height Analysis. Distribution of event amplitudes versus frequency of event occurrences.

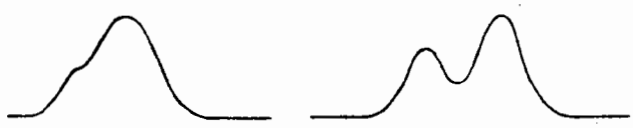
POLE/ZERO--A method of compensating the preamplifier's output signal fall time and the amplifier's shaping time constant. Its use improves the amplifier's high count rate resolution and overload recovery.



PULSE DECAY TIME--The time interval during which a pulse drops from its original peak amplitude to a stated fraction of its original amplitude.

PULSE PAIR RESOLUTION--The ability to discriminate between two pulses close together in time.

PULSE PILEUP--A condition where two succeeding pulses are so close together in time that the beginning of the second pulse occurs before the first pulse has returned to the baseline, thus giving the second pulse the appearance of a greater amplitude than it actually possesses.



Leading Edge Pileup Trailing Edge Pileup

PULSE PILEUP REJECTOR--An electronic circuit for sensing the pileup condition and rejecting the piled up (convoluted) pulses from processing.

RANGE, ADC--The full scale address of the ADC memory group.

REGION OF INTEREST--A user-determined area of the MCA display which contains data of particular interest, such as a peak.

RESOLUTION--The ability of an amplifier or a detector to differentiate between two peaks that are close together in energy. Thus, the narrower the peak, the better the resolution capability. Measured as FWHM.

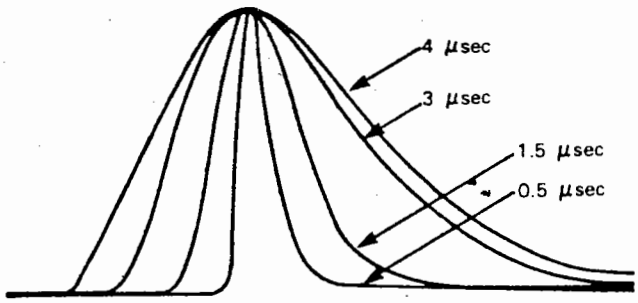
RESTORER (BASELINE RESTORATION)--A circuit usually used at the spectroscopy amplifier output to define a dc reference baseline (normally 0 volts).

ROI--See Region of Interest.

ROLL--The WINDOW function's ability to move through the displayed spectrum while retaining its original width (number of channels).

SCA--Single Channel Analyzer--recognizes events (pulses) that fall within two voltage limits (an LLD and a ULD) set by the operator. Outputs a logic pulse for each event recognized.

SHAPING--A process of modifying the input pulse shape to one more suitable for ADC processing.



SHV--Safe High Voltage connector.

SLOW NIM SIGNAL--See Logic Pulse.

SMOOTH--An MCA function where the data in one channel is averaged with data in adjacent channels in order to decrease or eliminate random data fluctuations.

SPECTRUM--A distribution of radiation intensity as a function of energy or time.

SPECTRUM BROADENING--A figure of merit indicative of overall system performance. Influenced by imperfections in the detection system, including detector ballistic deficit, system (electronic) noise and pulse pileup.

STRIP--An MCA function where an operator specified fractional part of the data in one section of memory is subtracted from the data in another section of memory. The data in the first section remain unchanged.

SYSTEM BUSY TIME--The Dead Time of an entire Spectroscopy System.

TERMINATOR--A load at the terminal end of a signal line.

THROUGHPUT--The capability of processing a unit of data in a specified time (for instance, in bits or pulses per second).

TIME TO PEAK--The time taken by a signal pulse to go from a specified level near the baseline (point of origin) to the pulse peak. See UNIPOLAR PULSE illustration.

TRANSFER--An MCA function where data in one section of memory can be copied into another section of memory without clearing data from the first section.

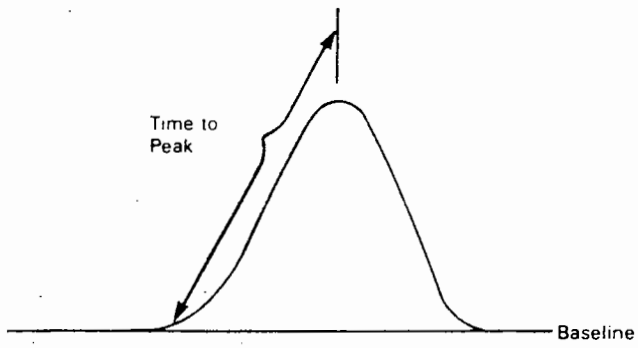
TRIGGER--A signal, usually a pulse, which initiates action in a circuit.

TRUE TIME--Real clock time.

TTL PULSE--See Logic Pulse.

ULD--Upper Level Discriminator - see LLD.

UNIPOLAR PULSE--A pulse that has an excursion in only one direction (either positive or negative) from the baseline.



WINDOW--An MCA function where a specific ROI is expanded to the full width of the display screen for close examination.

ZERO, ADC--The zero energy channel of the ADC, which is commonly aligned with channel zero of the memory. See OFFSET, ADC.

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FCC Warning:

WARNING:
This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

SERIES 35 PLUS
Schematics Package

SERIES 35 PLUS SCHEMATICS
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